

# Computer Systems and -architecture

## Project Exam Retake

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*Don't hesitate to contact the teaching assistant of this course. You can reach him in room M.G.305 or by e-mail.*

## Time Schedule

Projects are solved individually. Projects build on each other, to converge into a unified whole at the end of the semester. At the evaluation moment, you will present your solution by giving a demo and answering some questions.

You will submit a solution for all seven projects from the first semester, with the differences explained in this project description. Covering all seven projects, you submit one report by filling in `verslag.html` completely. A report typically consists of 1000 words and a number of drawings/screenshots. Put all your files in one `tgz` archive, as explained on the course's website, and submit your report to the exercises on Blackboard.

## Project

Extend your datapath to support data words (in register and data memory) of 16 bit. Aside from changes to the datapath itself, this will require changes to:

- ripple-carry adder and carry-lookahead adder
- ALU (and all ALU instructions)
- register and register file

The instruction set your datapath supports remains the same. Note that immediate instructions still only operate on the lower 6 bits, with the exception of the `lui` operation which operate on the upper 6 bits.

Make sure you use `TestRetake.py` for this project. As always, if you have questions about the script, cannot get it to work or suspect that there is a bug, contact the teaching assistant.