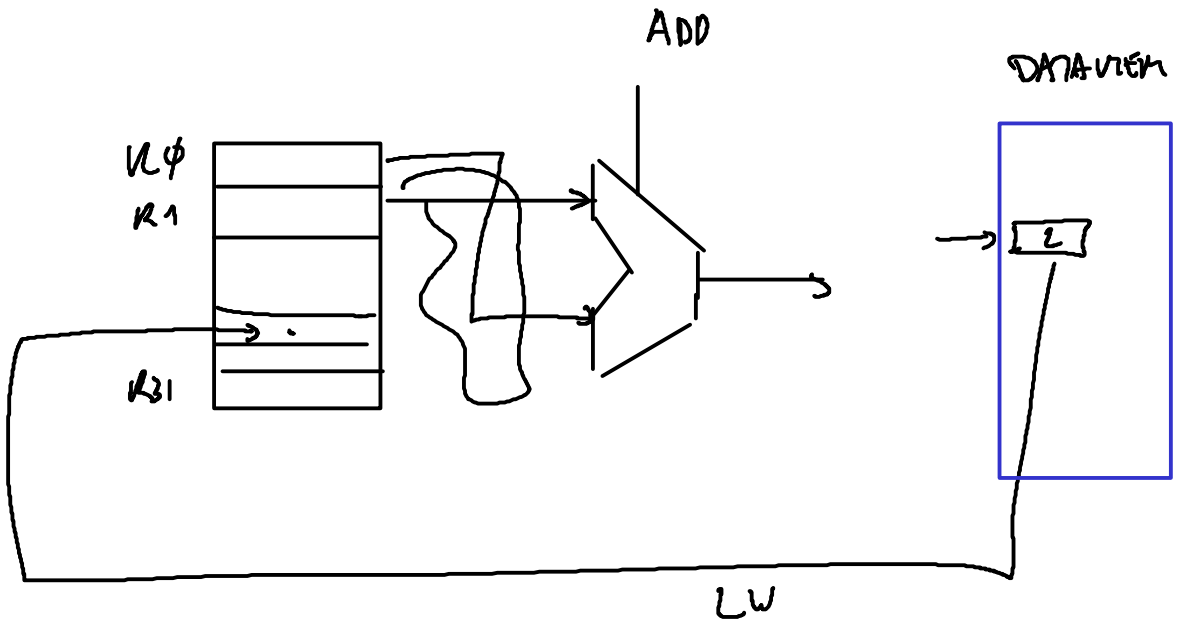


ADD $R5, $R7, $R10

+

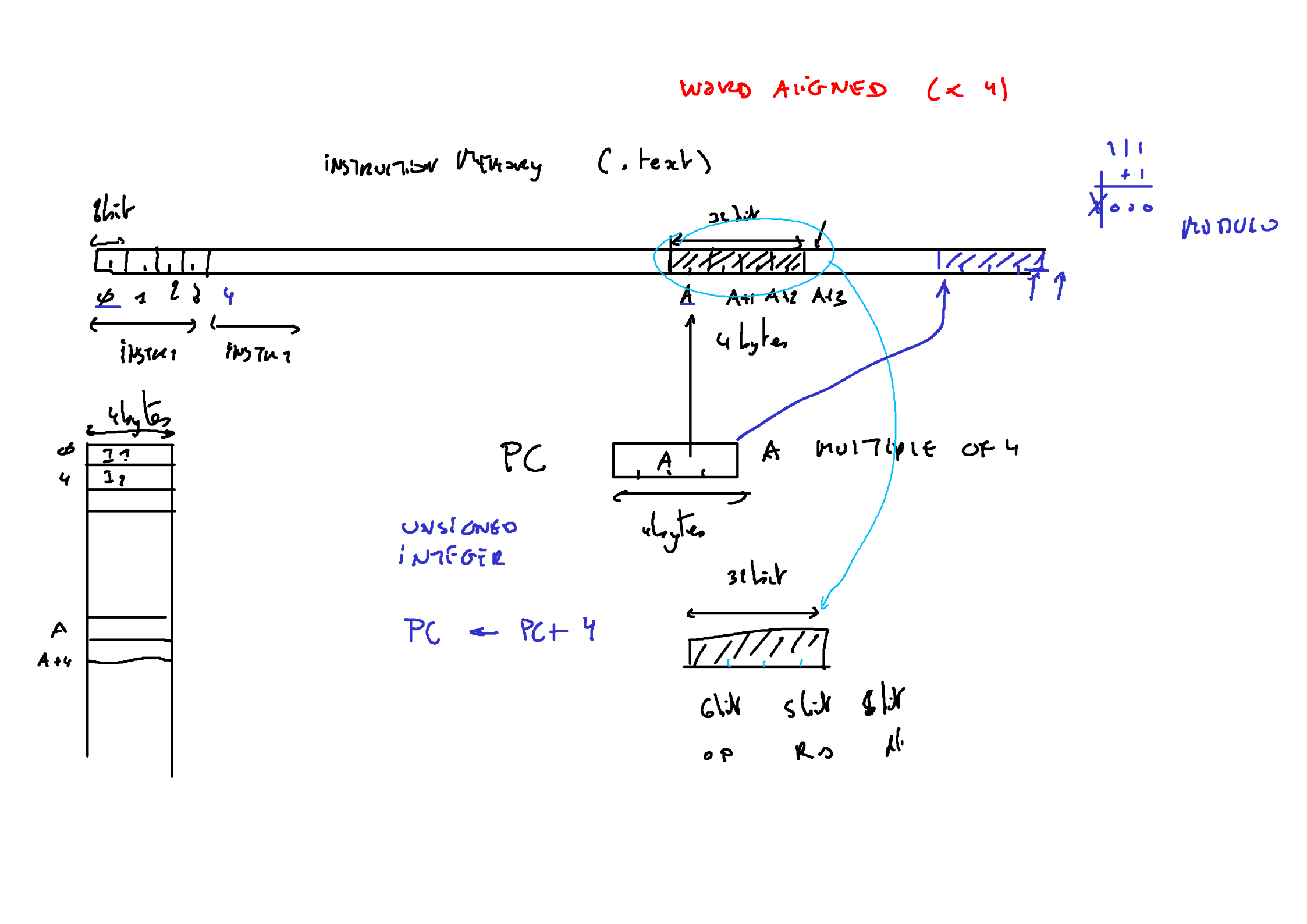
ADDI $R5, $R7, 2 ε

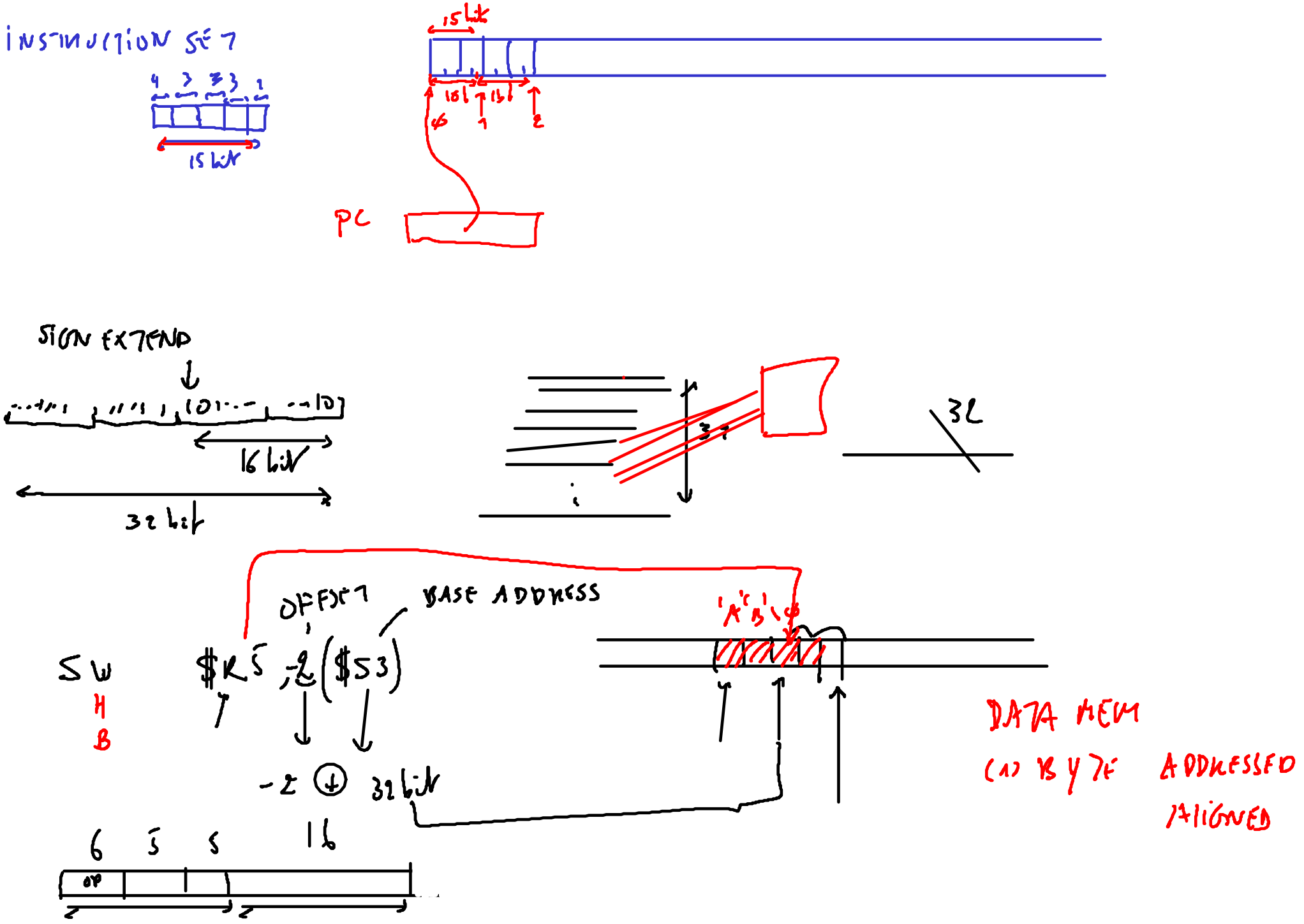
+

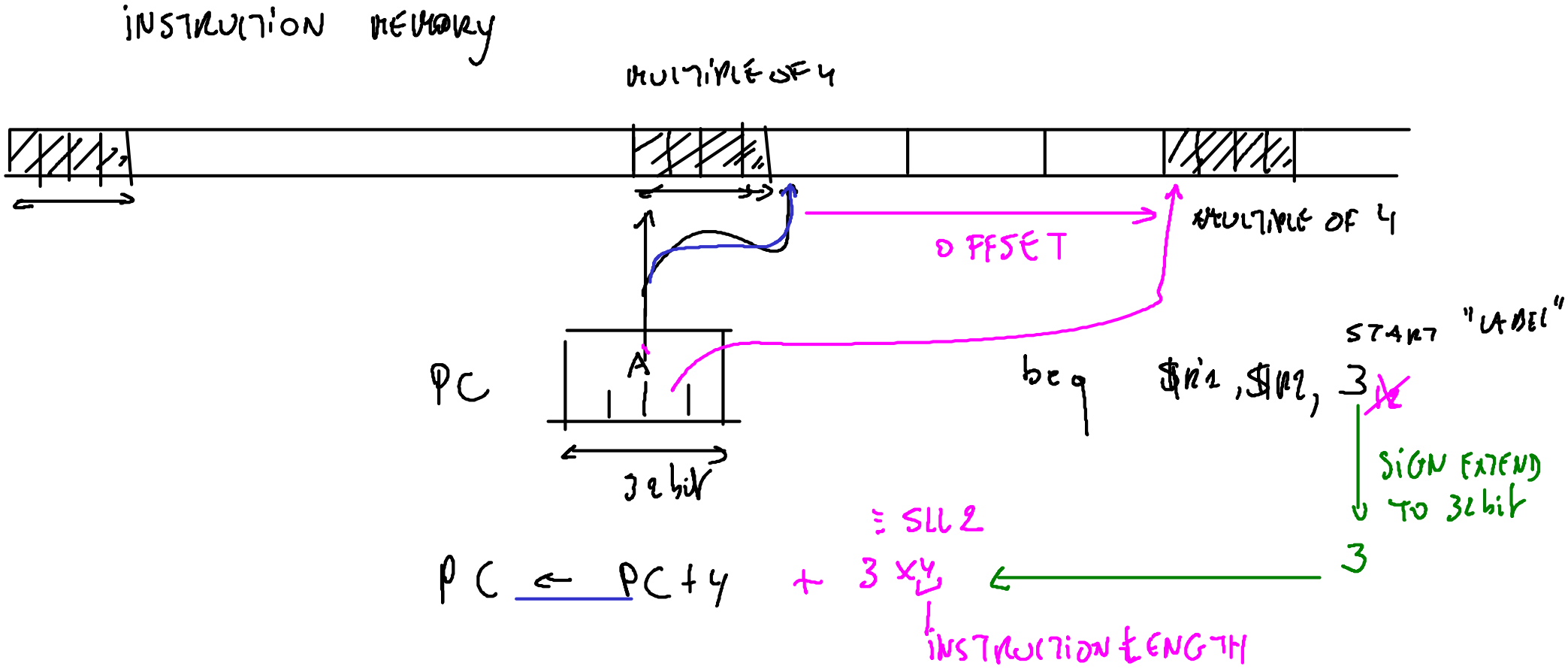
LW $R10, → ε 2

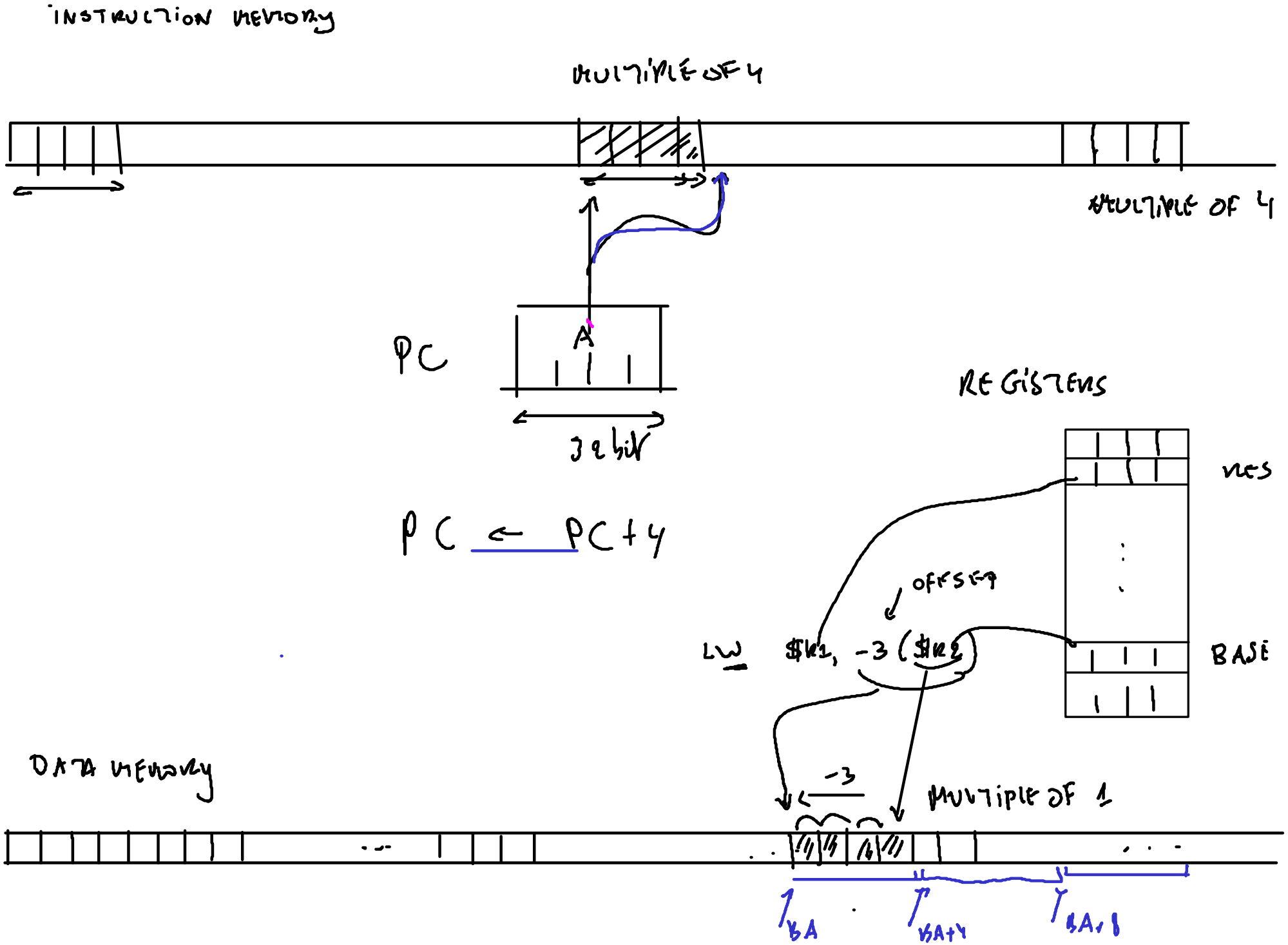
ADD $R5, $R7, $R10 ε

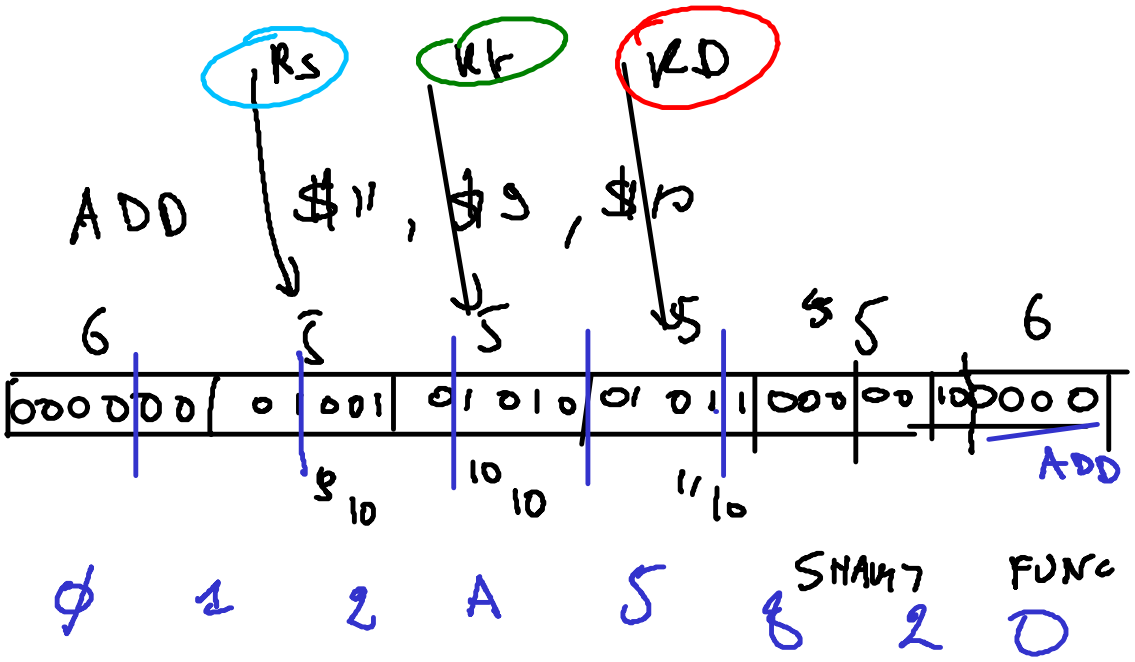
a += 1


WORD ALIGNED (x 4)
INSTRUCTION MEMORY (.text)
8 bit
32 bit
0 1 2 3 4
INSTR 1
INSTR 2
A A+1 A+2 A+3
4 bytes
MODULO
4 bytes
0
4
A
A+4
PC
A
A MULTIPLE OF 4
4 bytes
UNSIGNED INTEGER
PC ← PC + 4
32 bit
6 bit 5 bit 5 bit
op RS


INSTRUCTION SET
PC
SIGN EXTEND
16 bit
32 bit
3L
OFFSET
BASE ADDRESS
SW
$RS
-2
($S3)
-2
32 bit
16
DATA MEM
(1) BYTE ADDRESSED
ALIGNED


INSTRUCTION MEMORY
MULTIPLE OF 4
OFFSET
MULTIPLE OF 4
PC
A
32bit
START "LABEL"
beq $in1, $in2, 3
SIGN EXTEND TO 32bit
= SLL 2
PC ← PC+4 + 3 x 4
3
INSTRUCTION LENGTH


INSTRUCTION MEMORY
MULTIPLE OF 4
MULTIPLE OF 4
PC
A
32 bit
PC ← PC+4
REGISTERS
REGS
OFFSET
LW $R1, -3 ($R2)
BASE
DATA MEMORY
-3
MULTIPLE OF 1
BA
BA+4
BA+8



$\$t_3 \leftarrow \$t_1 + \$t_2$

ADD $\$t_3$, $\$t_1$, $\$t_2$

LW REG # , OFFSET (BASE REG #)

+/-

16 bit

CONTENT IS BASE ADDRESS

DATA MEM

$[-2^{15} \quad \ldots \quad +2^{15}-1]$

32 x 1024