Computer Systems and -architecture

Project 6: Full Datapath

1 Ba INF 2020-2021

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Don't hesitate to contact the teaching assistant of this course. You can reach him in room M.G.305 or by e-mail.

Time Schedule

Projects are solved in pairs of two students. Projects build on each other, to converge into a unified whole at the end of the semester. During the semester, you will be evaluated three times. At these evaluation moments, you will present your solution of the past projects by giving a demo and answering some questions. You will immediately receive feedback, which you can use to improve your solution for the following evaluations.

For every project, you submit a small report of the project you made by filling in `verslag.html` completely. A report typically consists of 500 words and a number of drawings/screenshots. Put all your files in one tgz archive, as explained on the course's website, and submit your report to the exercises on Blackboard.

- Report deadline: **December 20, 2020, 23u55**
- Evaluation and feedback: **December 21, 2020 - January 3, 2021**

Project

Read sections 4.1, 4.2, 4.3 and 4.4 of Chapter 4. You can use all Logisim libraries for this assignment.

1. In the previous assignment, we used the ALU operations as instructions and added two additional instructions (`lw` and `sw`). Next to these instructions, in this assignment we also support immediate instructions as well as branch and jump instructions.

   We introduce a number of new instructions, including instructions for `jump` and `branch`. Because you should be able to branch, you will have to connect your **program counter** to your datapath so that it can jump to a given address instead of just the next instruction.

   Implement the instructions described in the table below ("imm" stands for "immediate", "uns" stands for "unsigned" and "sig" stands for "signed, two's complement"). You already have implemented the R-type instructions and the lw/sw instructions in the previous assignment.

<table>
<tr><th>15</th><th>14</th><th>13</th><th>12</th><th>11</th><th>10</th><th>9</th><th>8</th><th>7</th><th>6</th><th>5</th><th>4</th><th>3</th><th>2</th><th>1</th><th>0</th><th>name</th><th>instruction</th><th>description</th></tr>
<tr><td colspan="4">0000</td><td colspan="4">rd</td><td colspan="4">0000</td><td colspan="4">0000</td><td>zero[1]</td><td><code>zero rd</code></td><td>$rd := 0</td></tr>
<tr><td colspan="4">0001</td><td colspan="4">rd</td><td colspan="4">rs</td><td colspan="4">0001</td><td>not[1]</td><td><code>not rd rs</code></td><td>$rd := !$rs</td></tr>
<tr><td colspan="4">0001</td><td colspan="4">rd</td><td colspan="4">rs</td><td colspan="4">1010</td><td>inv[1]</td><td><code>inv rd rs</code></td><td>$rd := -$rs</td></tr>
<tr><td colspan="4">0001</td><td colspan="4">rd</td><td colspan="4">rs</td><td colspan="4">1011</td><td>sll[1]</td><td><code>sll rd rs</code></td><td>$rd := $rs << 2</td></tr>
<tr><td colspan="4">0001</td><td colspan="4">rd</td><td colspan="4">rs</td><td colspan="4">1100</td><td>srl[1]</td><td><code>srl rd rs</code></td><td>$rd := $rs >> 2</td></tr>
<tr><td colspan="4">0001</td><td colspan="4">rd</td><td colspan="4">rs</td><td colspan="4">1101</td><td>sla[1]</td><td><code>sla rd rs</code></td><td>$rd := $rs * 2</td></tr>
<tr><td colspan="4">0001</td><td colspan="4">rd</td><td colspan="4">rs</td><td colspan="4">1110</td><td>sra[1,2]</td><td><code>sra rd rs</code></td><td>$rd := $rs / 2</td></tr>
<tr><td colspan="4">0001</td><td colspan="4">rd</td><td colspan="4">rs</td><td colspan="4">1111</td><td>cp[1]</td><td><code>cp rd rs</code></td><td>$rd := $rs</td></tr>
<tr><td colspan="4">0010</td><td colspan="4">rd</td><td colspan="4">rs</td><td colspan="4">rt</td><td>and[1]</td><td><code>and rd rs rt</code></td><td>$rd := $rs & $rt</td></tr>
<tr><td colspan="4">0011</td><td colspan="4">rd</td><td colspan="4">rs</td><td colspan="4">rt</td><td>or[1]</td><td><code>or rd rs rt</code></td><td>$rd := $rs | $rt</td></tr>
<tr><td colspan="4">0100</td><td colspan="4">rd</td><td colspan="4">rs</td><td colspan="4">rt</td><td>add[1]</td><td><code>add rd rs rt</code></td><td>$rd := $rs + $rt</td></tr>
<tr><td colspan="4">0101</td><td colspan="4">rd</td><td colspan="4">rs</td><td colspan="4">rt</td><td>sub[1]</td><td><code>sub rd rs rt</code></td><td>$rd := $rs - $rt</td></tr>
<tr><td colspan="4">0110</td><td colspan="4">rd</td><td colspan="4">rs</td><td colspan="4">rt</td><td>lt[1]</td><td><code>lt rd rs rt</code></td><td>$rd := $rs < $rt ? 1 : 0</td></tr>
<tr><td colspan="4">0111</td><td colspan="4">rd</td><td colspan="4">rs</td><td colspan="4">rt</td><td>gt[1]</td><td><code>gt rd rs rt</code></td><td>$rd := $rs > $rt ? 1 : 0</td></tr>
<tr><td colspan="4">1000</td><td colspan="4">rd</td><td colspan="4">rs</td><td colspan="4">rt</td><td>eq[1]</td><td><code>eq rd rs rt</code></td><td>$rd := $rs = $rt ? 1 : 0</td></tr>
<tr><td colspan="4">1001</td><td colspan="4">rd</td><td colspan="4">rs</td><td colspan="4">rt</td><td>neq[1]</td><td><code>neq rd rs rt</code></td><td>$rd := $rs != $rt ? 1 : 0</td></tr>
<tr><td colspan="4">1010</td><td colspan="4">rd</td><td colspan="4">rs</td><td colspan="4">imm (signed)</td><td>lw</td><td><code>lw rd rs imm</code></td><td>$rd := MEM[$rs+imm]</td></tr>
<tr><td colspan="4">1011</td><td colspan="4">rd</td><td colspan="4">rs</td><td colspan="4">imm (signed)</td><td>sw</td><td><code>sw rd rs imm</code></td><td>MEM[$rs+imm] := $rd</td></tr>
<tr><td colspan="4">1100</td><td colspan="4">rd</td><td colspan="8">unsigned immediate</td><td>ori</td><td><code>ori rd imm</code></td><td>$rd := $rd | imm</td></tr>
<tr><td colspan="4">1101</td><td colspan="4">rd</td><td colspan="8">unsigned immediate</td><td>lui</td><td><code>lui rd imm</code></td><td>$rd := imm << 8</td></tr>
<tr><td colspan="4">1110</td><td colspan="4">rd</td><td colspan="8">immediate (signed)</td><td>brnz</td><td><code>brnz rd imm</code></td><td>$rd != 0 ? $pc := $pc + 1 + imm</td></tr>
<tr><td colspan="4">1111</td><td colspan="8">target address</td><td colspan="4">0000</td><td>j</td><td><code>j imm</code></td><td>$pc := addr</td></tr>
<tr><td colspan="4">1111</td><td colspan="4">rd</td><td colspan="4">immediate (signed)</td><td colspan="4">0100</td><td>jr</td><td><code>jr rd imm</code></td><td>$pc := $rd + imm</td></tr>
<tr><td colspan="4">1111</td><td colspan="8">target address</td><td colspan="4">1111</td><td>jal[3]</td><td><code>jal imm</code></td><td>$r15 := $pc + 1; $pc := addr</td></tr>
</table>

[1] R-type instruction.

[2] Integer division.

[3] Register r15 will be reserved for the return address of the `jal` instruction.

- In order to get all control lines right, you will have to add a **Control Unit** circuit to your datapath.
  - Input is the instruction (16 bits).
  - Outputs are the ALU OP-code as well as all control lines for i.e. the program counter, instruction and data memory, multiplexers and the register file. Choose your control lines wisely: this can make the implementation a lot easier!

  More information on the implementation of a control unit can be found in Section 4.4 of *Computer organization and design.*
- Similarly you can create an **Immediate** circuit (this is different from the book's datapath):
  - Input is the instruction (16 bits).
  - Output is the immediate value (16 bits), depending on the instruction this will be a 4 or 8-bit value that is unsigned/sign extended/shifted to 16 bits.
- Once done, your datapath can correctly execute a program written in machine language, as the behaviour of arithmetic, branching and memory operations is now fully implemented! You can use the script `Test.py` as follows (note the `-f` flag to denote the simulation of a full datapath:

  ```
  python Test.py -f -t <test-file> -c <circ-file>
  ```

  You can use labels for branching and jumping in your tests. When testing the full datapath, you can only perform checks at the end of the program. (This is because of branching: it would not make sense to check a register value in the middle of a loop, as it can have a different value in a different iteration of the loop.)
- To prepare for the next lab session, read section 4.9 of Chapter 4.