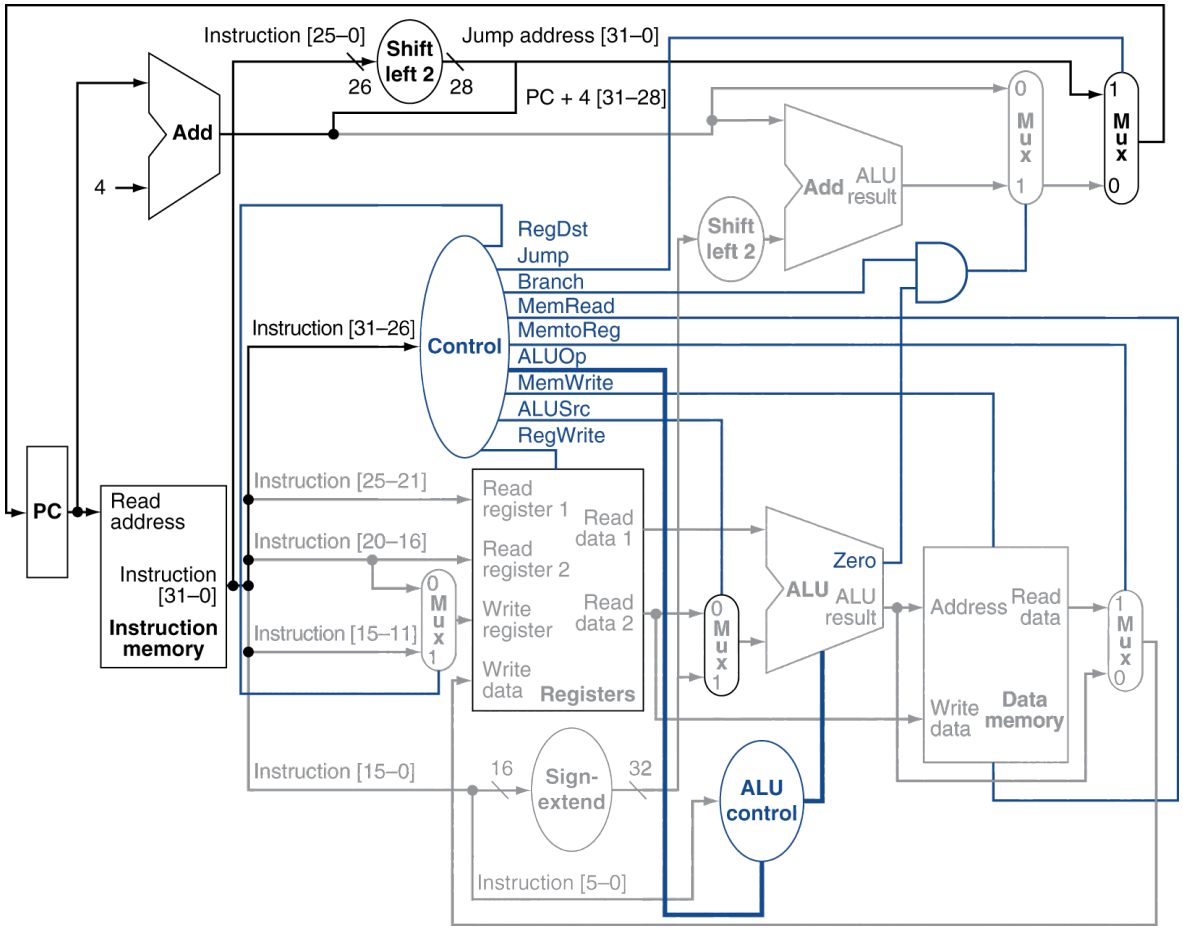
The Processor

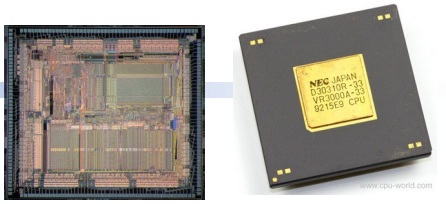
Designing the **datapath**



Program Execution (performance)

- Algorithm
  - Determines **number of operations** executed
- Programming language, compiler, architecture (Instruction Set Architecture – ISA)
  - Determine number of **machine instructions** executed **per operation** (clock Cycles Per Instruction – CPI)
- Processor and memory system
  - Determine **how fast instructions** are **executed** (cycle time)
- I/O system (and OS)
  - Determines **how fast I/O operations** are **executed**

Program Execution



32 bit MIPS R3000 processor (115000 transistors) early 1990s

- We will examine two MIPS hardware implementations (aka “datatpath”) with identical ISAs:
  - A simplified version
  - A more realistic pipelined version (**I**nstruction-**L**evel **P**arallellism)
- We will subsequently introduce “exception” handling and what this requires in the datapath
- Simple (but sufficient) subset, only essential instructions

  Different types of instructions (Instruction Set):
  - Memory access: `lw, sw`
  - Arithmetic/logical: `add, sub, and, or, slt`
  - Control transfer: `beq, j`

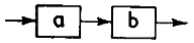
Böhm – Jacopini theorem

The “structured program” theorem (from programming language theory):

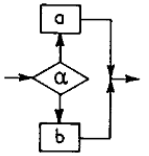
Böhm, Corrado and Jacopini, Giuseppe (1966).
”Flow Diagrams, Turing Machines and Languages with only Two Formation Rules”. Communications of the ACM 9(5):366-371.
http://www.cs.unibo.it/~martini/PP/bohm-jac.pdf

A class of control flow graphs can compute any computable function (algorithm) if it combines subprograms in only three specific ways (*i.e.,* by means of only three control structures):

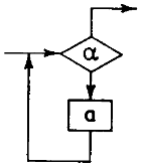
1) Executing one subprogram, and then another subprogram (sequence)



2) Executing one of two subprograms according to the value of a Boolean expression (selection)

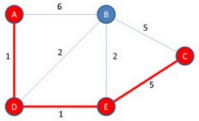


3) Repeatedly executing a subprogram as long as a Boolean expression is true (iteration)



Note: assembly/machine code is not “structured” HLL (as it uses **Go To**).

Edsger Dijkstra (1968).
"**Go To** Statement Considered Harmful". Communications of the ACM. 11 (3): 147–148.
https://homepages.cwi.nl/~storm/teaching/reader/Dijkstra68.pdf



Frank Rubin (1987).
""GOTO Considered Harmful" Considered Harmful". Communications of the ACM. 30 (3): 195–196.
http://www.ecn.purdue.edu/ParaMount/papers/rubin87goto.pdf

""GOTO Considered Harmful" Considered Harmful' Considered Harmful?" ...

Instruction Set Architecture (ISA)

Special Architectures:

- (Super) vector computers
- GPU (matrix operations)
- Special purpose (signal processing, ECU, ...)

Instruction Set Architecture (ISA)

Design Principles (HW/SW):

1. Regularity
2. Smaller is Faster
3. Make the Common Case Fast
4. Good Design demands Good Compromises

Instruction Set Architecture (ISA)

Different instruction **types**:

Memory access: `lw, sw`
Arithmetic/logical: `add, sub, and, or, slt`
Control transfer: `beq, j`

Different instruction **instances**:

```
add    $s1, $s2, $s3
add    $s1, $s1, $s2
add    $s1, $s1, $s1
```

Different instruction (encoding) **formats**:

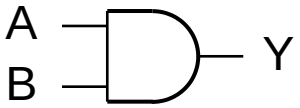
Name	Fields						Comments
Field size	6 bits	5 bits	5 bits	5 bits	5 bits	6 bits	All MIPS instructions are 32 bits long
R-format	op	rs	rt	rd	`shamt`	funct	Arithmetic instruction format
I-format	op	rs	rt	address/immediate			Transfer, branch, `imm`. format
J-format	op	target address					Jump instruction format

Logic Design Basics (recap)

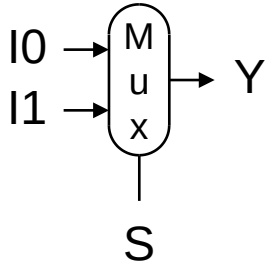
- Information encoded in **bi**nary digi**ts**
  - Low voltage = 0, High voltage = 1 (or reverse)
  - One wire per bit
  - Multi-bit data encoded on multi-wire **buses**
- **Combinational** element
  - **Operate** on **data**
  - Output is a **function** of input
- **State** (**sequential**) elements
  - **Store/Hold/Retrieve** information

Combinational Elements

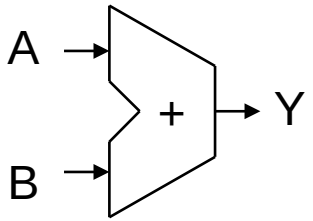
- AND-gate
  - Y = A & B



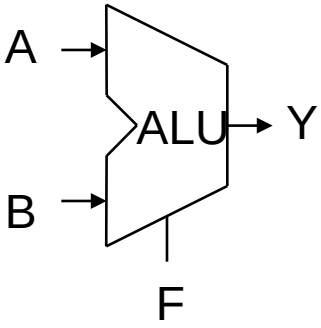
- Multiplexer
  - Y = S ? I1 : I0



- Adder
  - Y = A + B



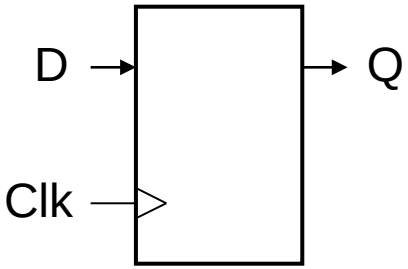
- Arithmetic/Logic Unit
  - Y = F(A, B)

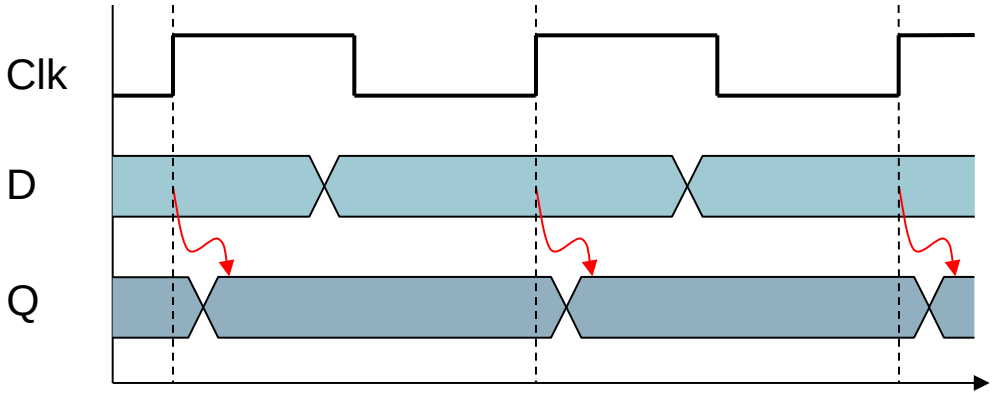


Sequential Elements

Register: stores data in a memory circuit

- Uses a clock signal Clk to determine **when** to **update** the **stored** value Q with D
- (rising/falling) **Edge-triggered**: **update** data in memory **when** Clk changes (from 0 to 1/1 to 0)

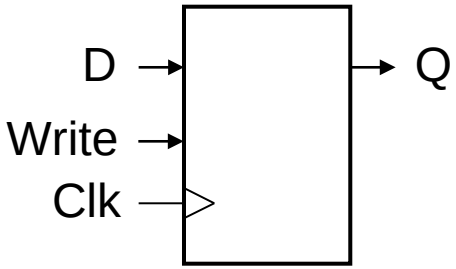


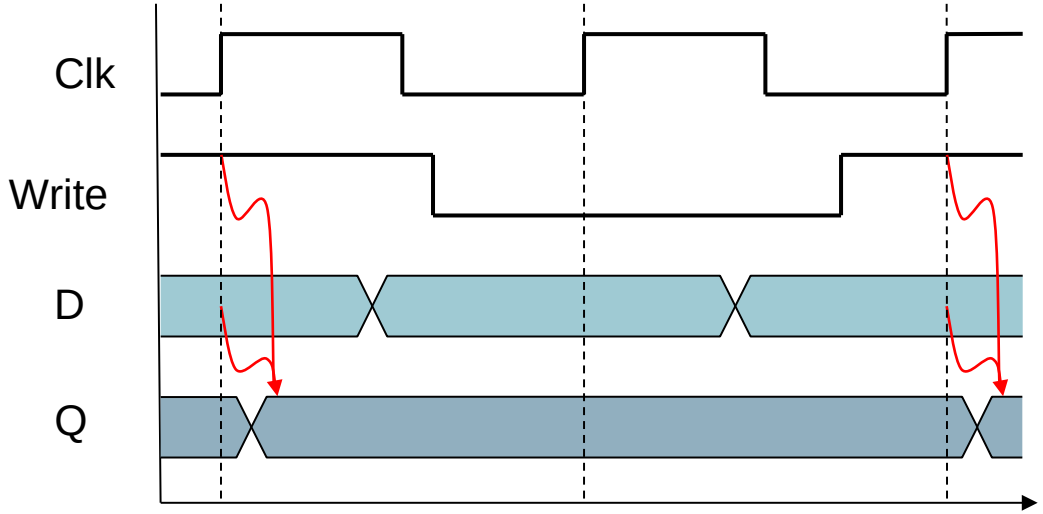


Sequential Elements

Register with **write control**

- Only updates on **clock edge**
  only when **write control input is 1**
- Used when stored value is to be kept over **multiple** clock cycles

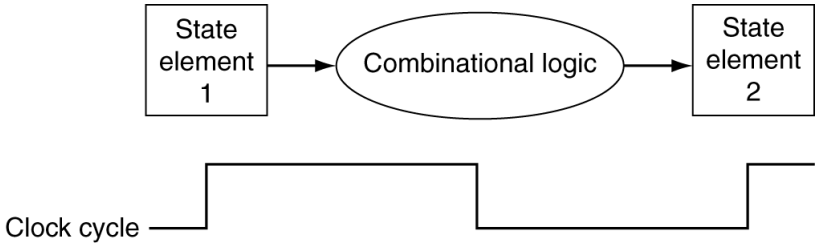


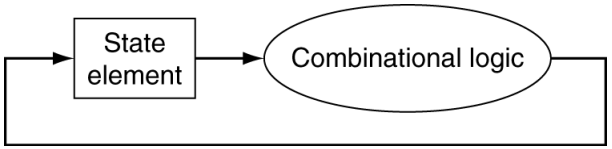


Clocking Methodology

Combinational logic
transforms data **during** clock cycles

- Between clock edges
- Input from state elements,
  Output to state element
- **Longest delay** due to combinational logic (implementing ISA “instructions”) determines **minimum** required **clock period**





Executing Machine Instructions

```
1          .data
2
3  values: .word   10
4          .word   12
5  result: .word   9
6
7          .text
8  start:
9
10 # ALU operations
11         li   $t1, 1
12         li   $t2, 2
13         add  $t3, $t1, $t2
14
15 # memory operations
16         la   $t0, values
17         lw   $t1, 0($t0)
18         lw   $t2, 4($t0)
19         add  $t3, $t1, $t2
20         la   $t0, result
21         sw   $t3, 0($t0)
22
23 # control flow
24         beq  $t3, $t3, start
25         addi $t3, $t3, 2
26
27         j    start
```

Executing Machine Instructions

Registers | Coproc 1 | Coproc 0

Name	Number	Value
$zero	0	0x00000000
$at	1	0x00000000
$v0	2	0x00000000
$v1	3	0x00000000
$a0	4	0x00000000
$a1	5	0x00000000
$a2	6	0x00000000
$a3	7	0x00000000
$t0	8	0x00000000
$t1	9	0x00000000
$t2	10	0x00000000
$t3	11	0x00000000
$t4	12	0x00000000
$t5	13	0x00000000
$t6	14	0x00000000
$t7	15	0x00000000
$s0	16	0x00000000
$s1	17	0x00000000
$s2	18	0x00000000
$s3	19	0x00000000
$s4	20	0x00000000
$s5	21	0x00000000
$s6	22	0x00000000
$s7	23	0x00000000
$t8	24	0x00000000
$t9	25	0x00000000
$k0	26	0x00000000
$k1	27	0x00000000
$gp	28	0x10008000
$sp	29	0x7fffeffc
$fp	30	0x00000000
$ra	31	0x00000000
pc		0x00400000
hi		0x00000000
lo		0x00000000

Executing Machine Instructions

Text Segment

Bkpt	Address	Code	Basic	Source
	0x00400000	0x24090001	addiu $9,$0,0x00000001	11: li $t1, 1
	0x00400004	0x240a0002	addiu $10,$0,0x0000...	12: li $t2, 2
	0x00400008	0x012a5820	add $11,$9,$10	13: add $t3, $t1, $t2
	0x0040000c	0x3c011001	lui $1,0x00001001	16: la $t0, values
	0x00400010	0x34280000	ori $8,$1,0x00000000	
	0x00400014	0x8d090000	lw $9,0x00000000($8)	17: lw $t1, 0($t0)
	0x00400018	0x8d0a0004	lw $10,0x00000004($8)	18: lw $t2, 4($t0)
	0x0040001c	0x012a5820	add $11,$9,$10	19: add $t3, $t1, $t2
	0x00400020	0x3c011001	lui $1,0x00001001	20: la $t0, result
	0x00400024	0x34280008	ori $8,$1,0x00000008	
	0x00400028	0xad0b0000	sw $11,0x00000000($8)	21: sw $t3, 0($t0)
	0x0040002c	0x116bfff4	beq $11,$11,0xfffffff4	24: beq $t3, $t3, start
	0x00400030	0x216b0002	addi $11,$11,0x0000...	25: addi $t3, $t3, 2
	0x00400034	0x08100000	j 0x00400000	27: j start

Executing Machine Instructions

Text Segment

Bkpt	Address	Code	Basic	Source
	0x00400000	0x24090001	addiu $9,$0,0x00000001	11: li $t1, 1
	0x00400004	0x240a0002	addiu $10,$0,0x0000...	12: li $t2, 2
	0x00400008	0x012a5820	add $11,$9,$10	13: add $t3, $t1, $t2
	0x0040000c	0x3c011001	lui $1,0x00001001	16: la $t0, values
	0x00400010	0x34280000	ori $8,$1,0x00000000	
	0x00400014	0x8d090000	lw $9,0x00000000($8)	17: lw $t1, 0($t0)
	0x00400018	0x8d0a0004	lw $10,0x00000004($8)	18: lw $t2, 4($t0)
	0x0040001c	0x012a5820	add $11,$9,$10	19: add $t3, $t1, $t2
	0x00400020	0x3c011001	lui $1,0x00001001	20: la $t0, result
	0x00400024	0x34280008	ori $8,$1,0x00000008	
	0x00400028	0xad0b0000	sw $11,0x00000000($8)	21: sw $t3, 0($t0)
	0x0040002c	0x116bfff4	beq $11,$11,0xfffffff4	24: beq $t3, $t3, start
	0x00400030	0x216b0002	addi $11,$11,0x0000...	25: addi $t3, $t3, 2
	0x00400034	0x08100000	j 0x00400000	27: j start

Labels

Label	Address ▲
tst.asm	
start	0x00400000
values	0x10010000
result	0x10010008

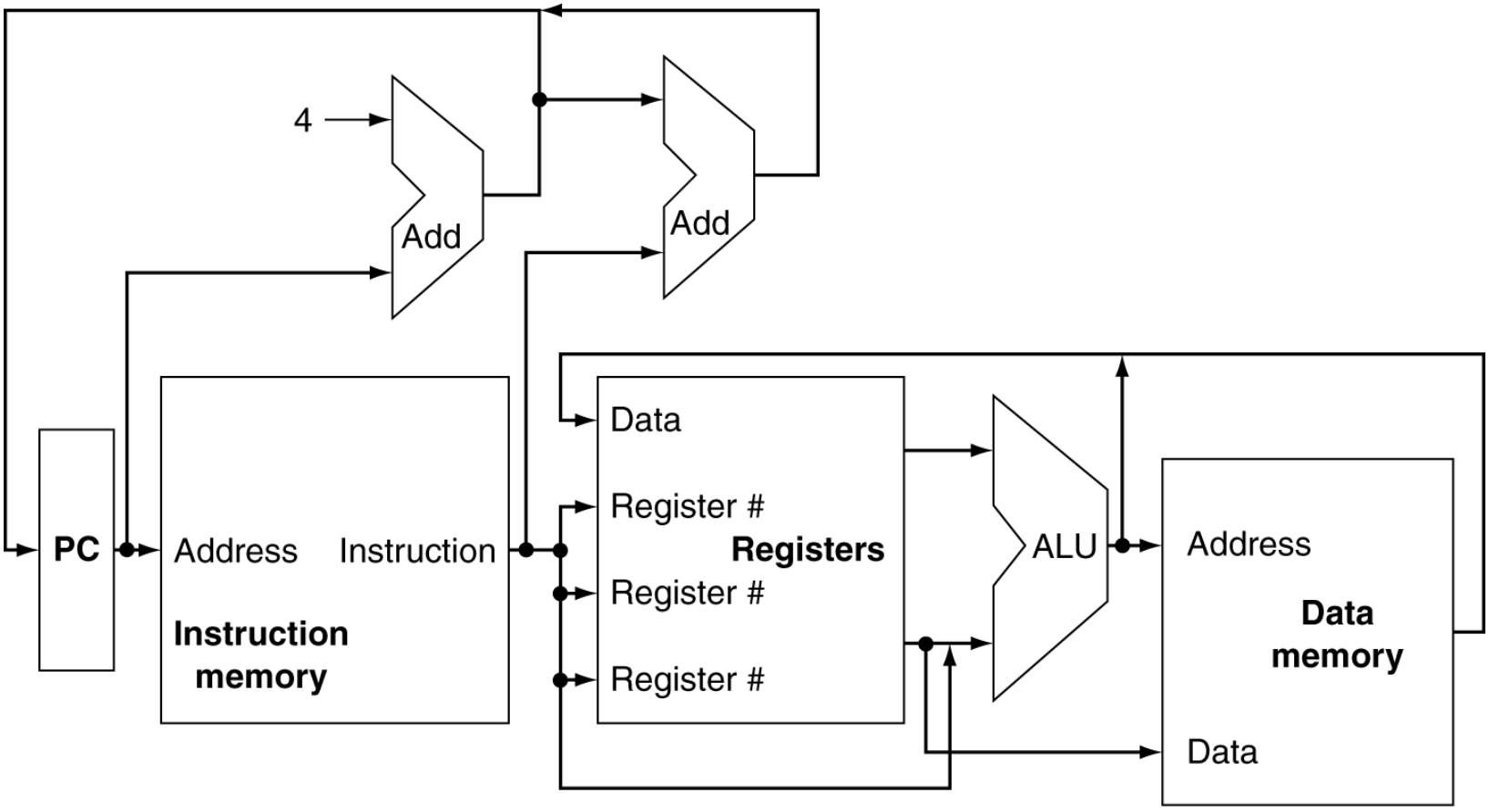
Data Segment

Address	Value (+0)	Value (+4)	Value (+8)	Value (+c)	Value (+10)	Value (+14)	Value (+18)	Value (+1c)
0x10010000	0x0000000a	0x0000000c	0x00000009	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010020	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010040	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010060	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010080	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x100100a0	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x100100c0	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x100100e0	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010100	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010120	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010140	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010160	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010180	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x100101a0	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x100101c0	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x100101e0	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000

Instruction Execution

- **PC** → instruction memory, **fetch** instruction
- Register numbers → **register file**, **read** registers
- Depending on **instruction type (class)**
  - Use **ALU** to calculate
    - Arithmetic result
    - Memory address for load/store
    - Branch target address
  - Access data **memory** for load/store
  - **PC** ← **PC + 4** (“next sequential instruction”) or **target address**

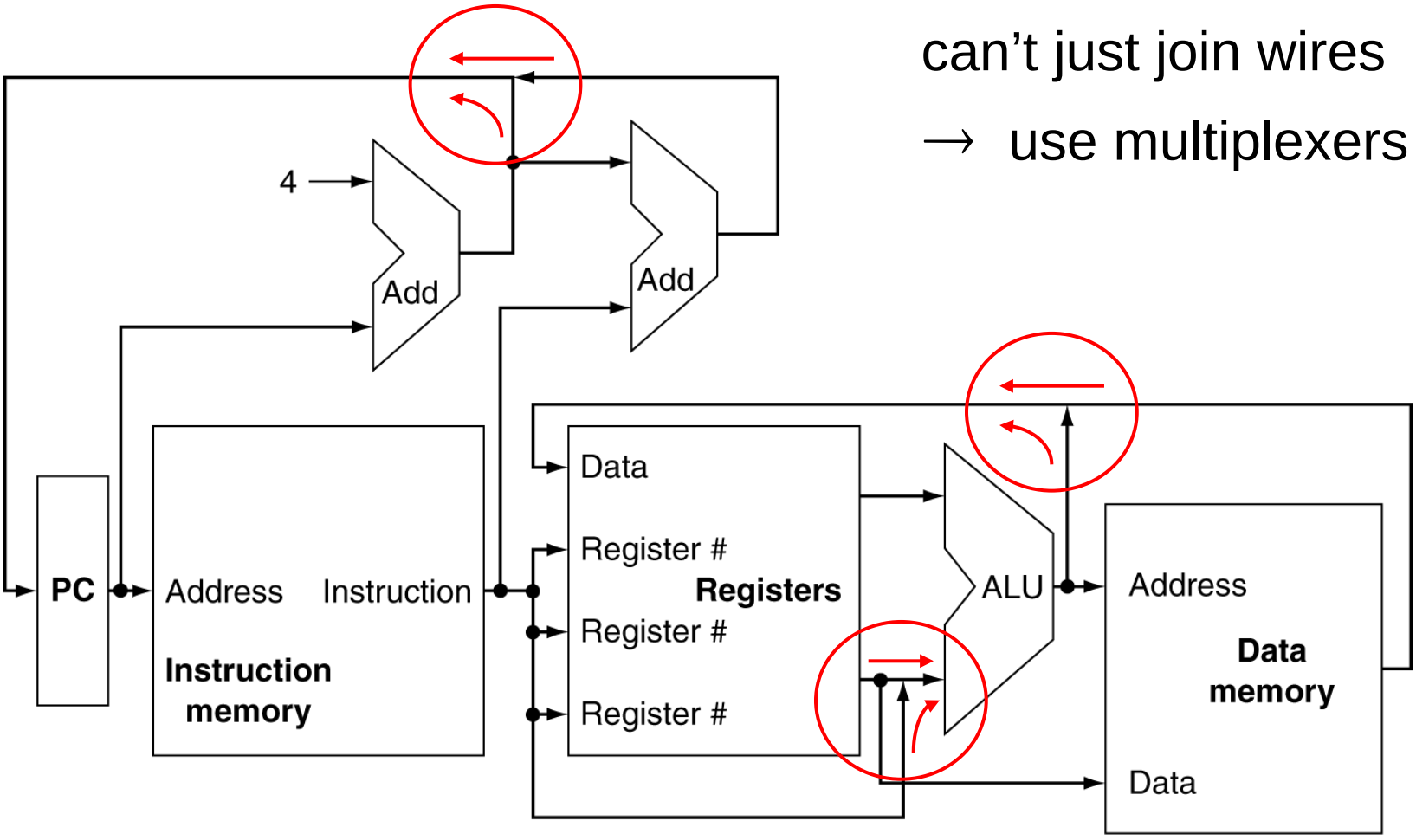
CPU Overview



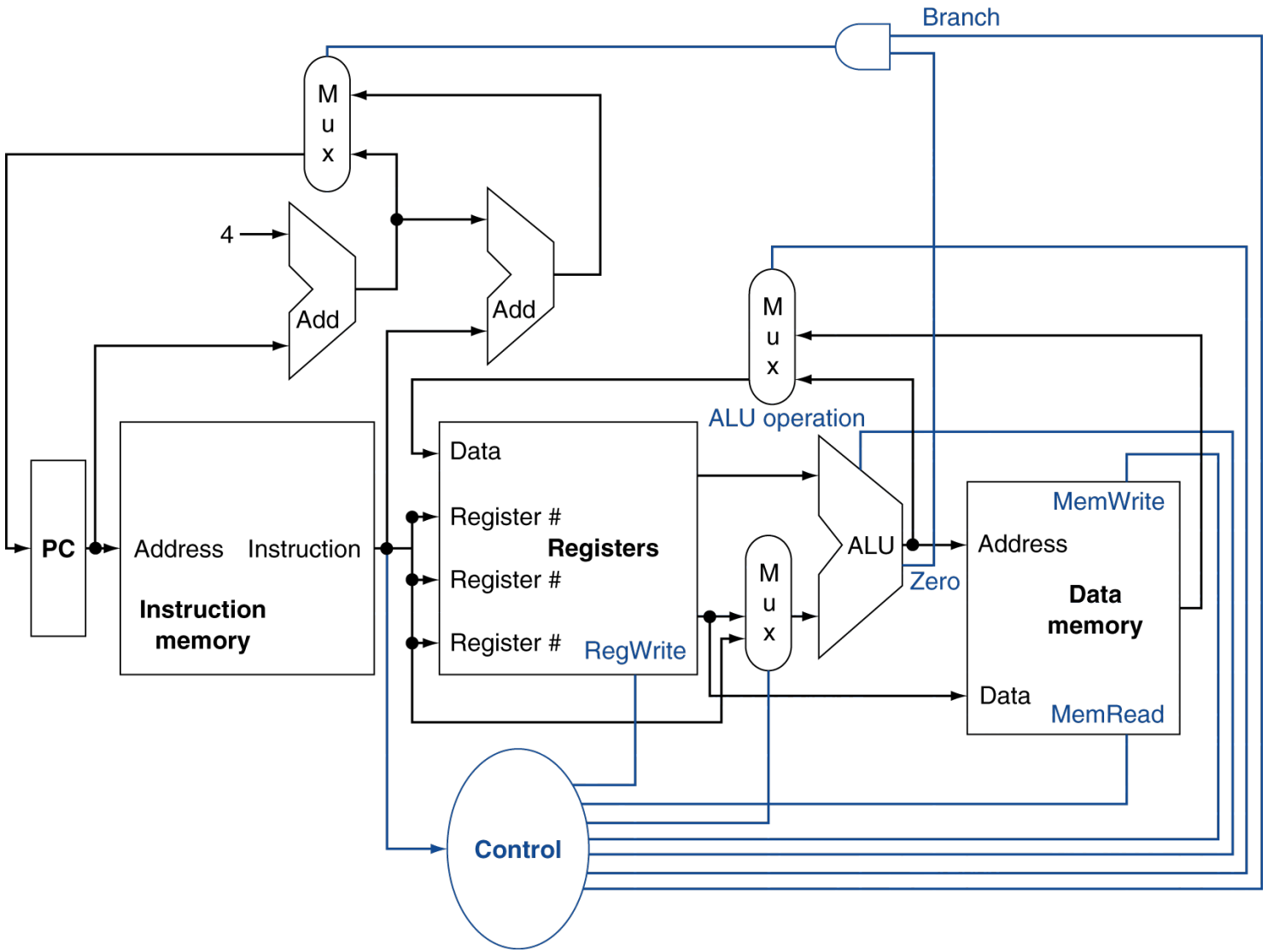
Multiplexers

can’t just join wires

→ use multiplexers



Control


Branch
M
u
x
4
Add
Add
M
u
x
ALU operation
PC
Address
Instruction
Instruction
memory
Data
Register #
Registers
Register #
Register #
RegWrite
M
u
x
ALU
Zero
MemWrite
Address
Data
memory
Data
MemRead
Control

Building a Datapath

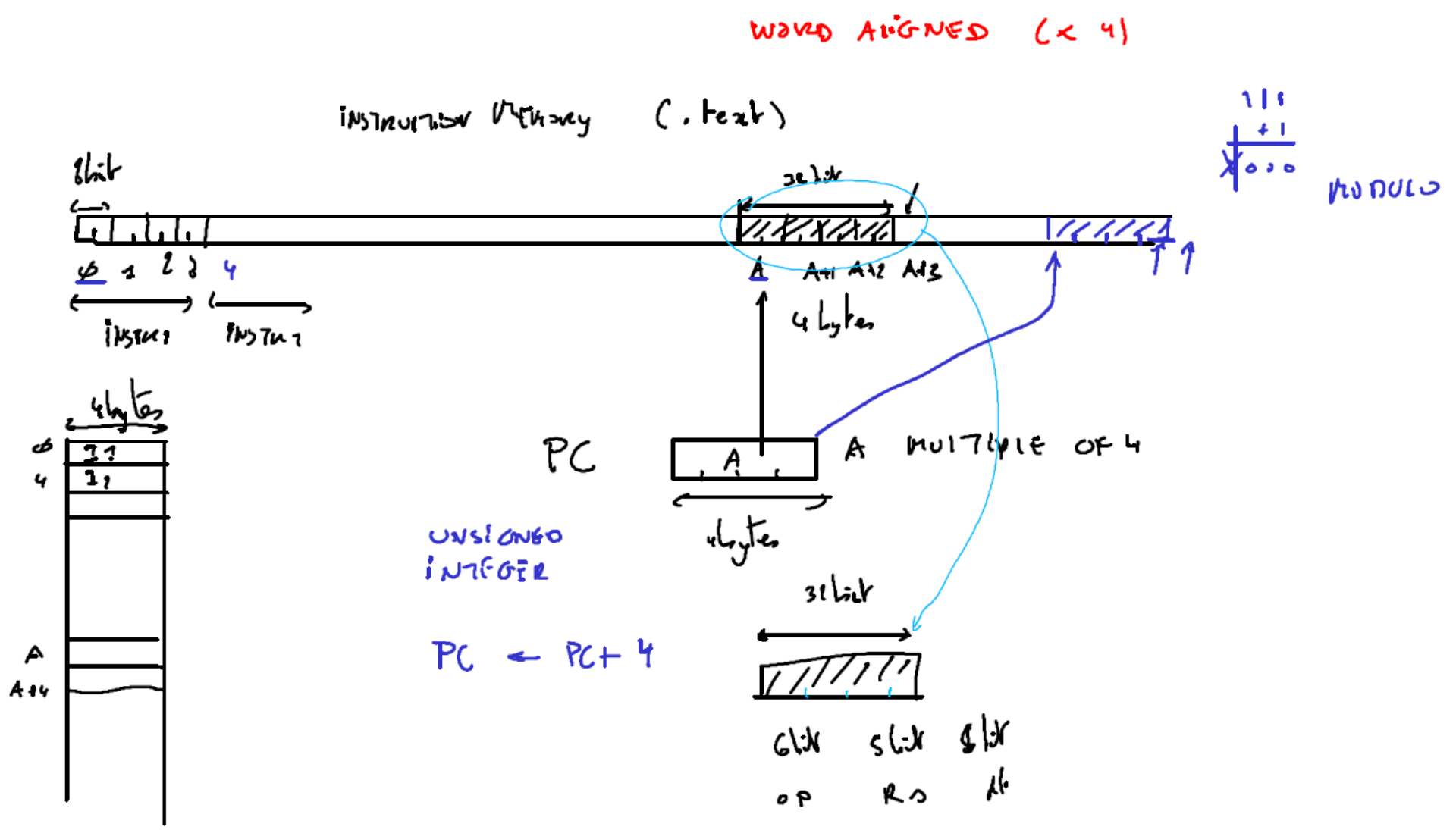
- Datapath =

  CPU **hardware architecture**
  that processes **instructions** and **data**

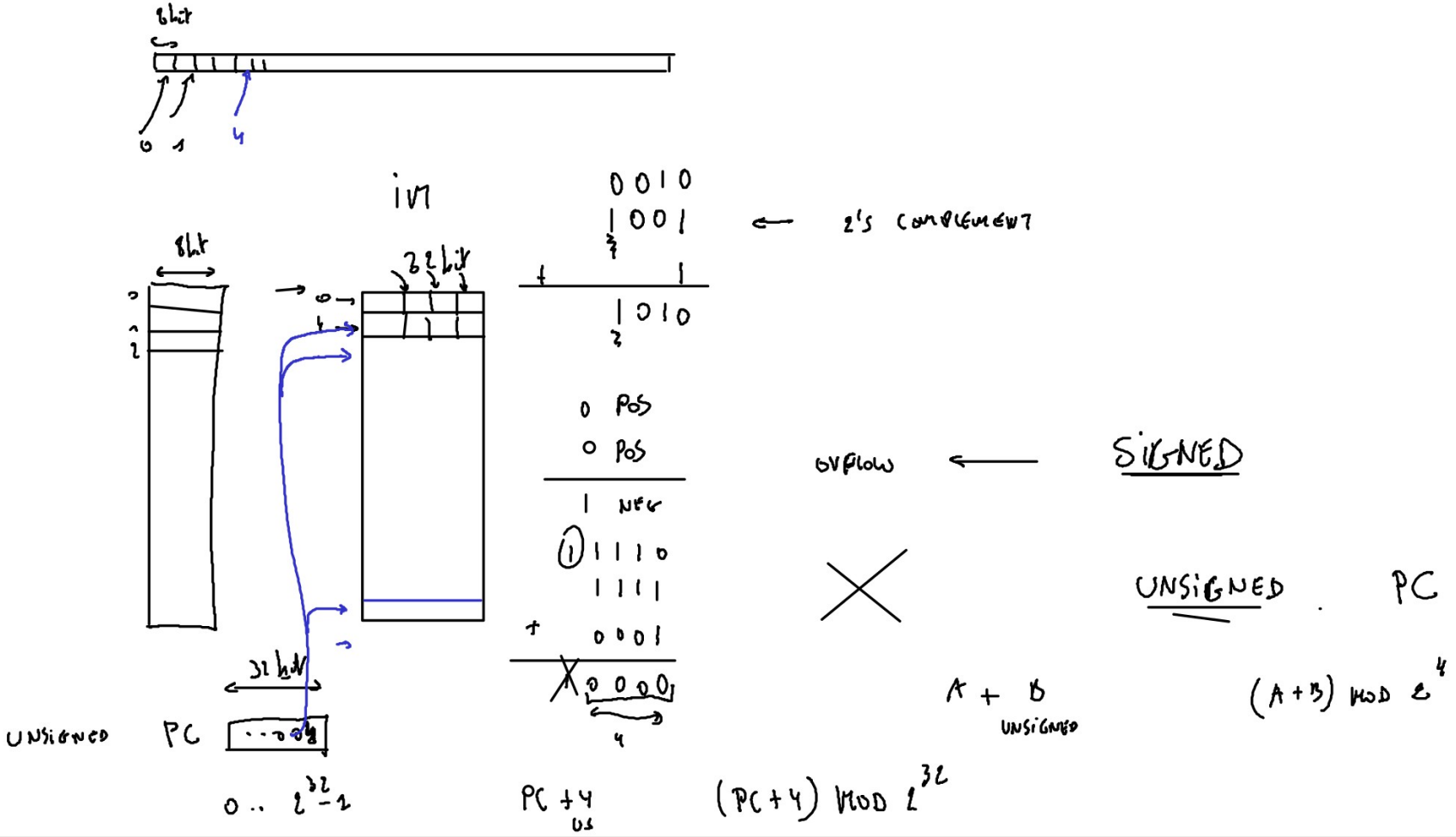
  - registers, ALUs, multiplexers, memories

- We will build a simplified MIPS datapath incrementally, refining the overview design

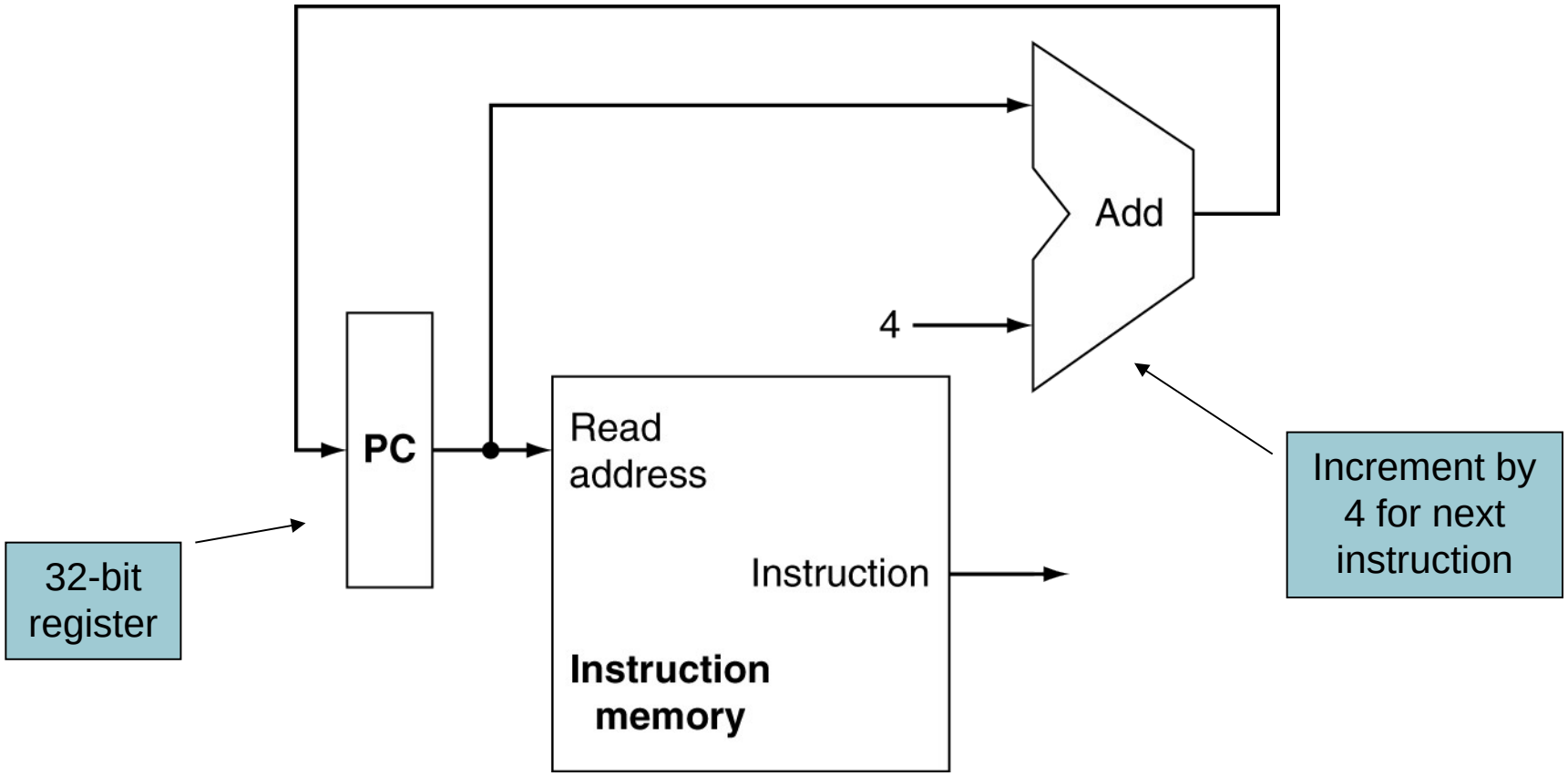
Instruction Fetch



Program Counter (PC) is unsigned



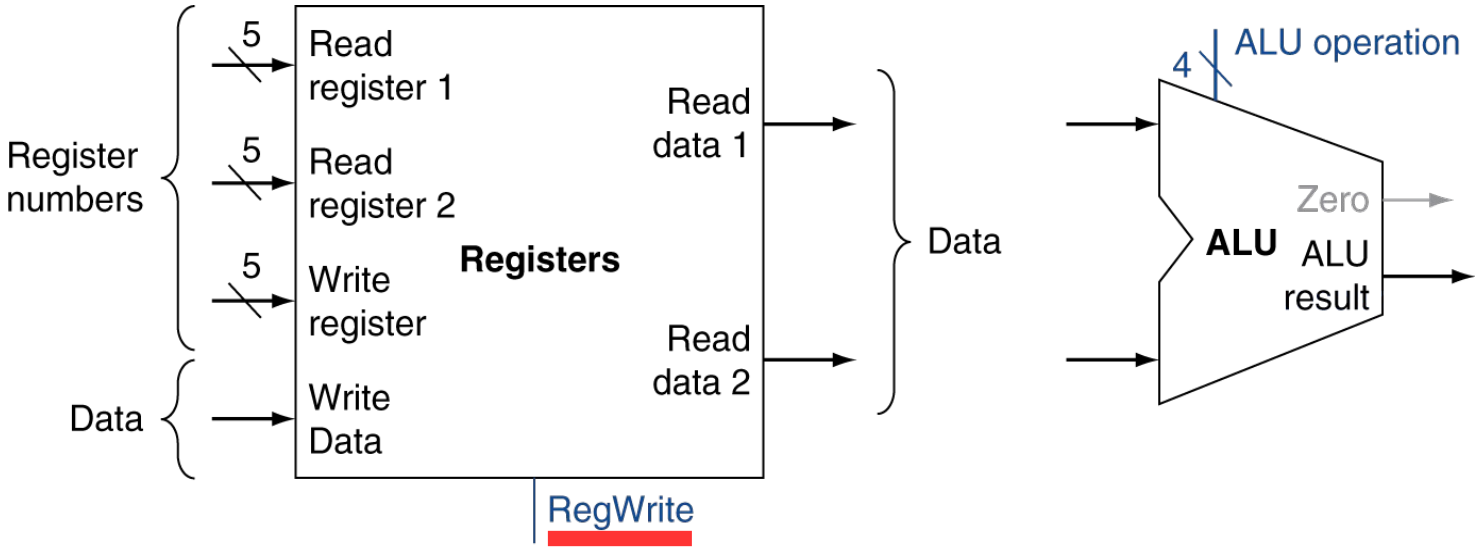
Instruction Fetch



R-Format Instructions

Name	Fields						Comments
Field size	6 bits	5 bits	5 bits	5 bits	5 bits	6 bits	All MIPS instructions are 32 bits long
R-format	op	rs	rt	rd	shamt	funct	Arithmetic instruction format
I-format	op	rs	rt	address/immediate			Transfer, branch, imm. format
J-format	op	target address					Jump instruction format

- Read two register operands
- Perform arithmetic/logical operation
- Write register result



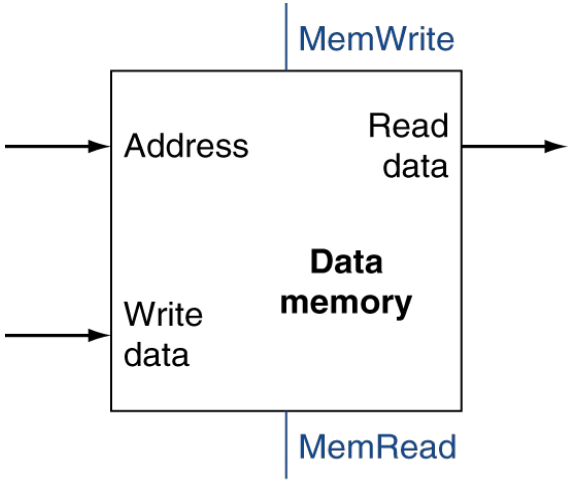
a. Registers

b. ALU

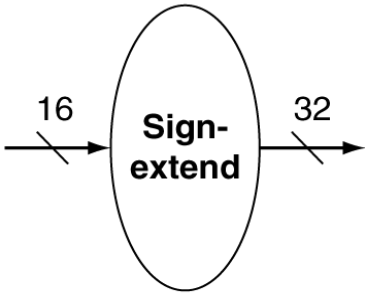
Load/Store Instructions

Name	Fields						Comments
Field size	6 bits	5 bits	5 bits	5 bits	5 bits	6 bits	All MIPS instructions are 32 bits long
R-format	op	rs	rt	rd	shamt	funct	Arithmetic instruction format
I-format	op	rs	rt	address/immediate			Transfer, branch, imm. format
J-format	op	target address					Jump instruction format

- Read register operands
- Calculate address using 16-bit offset
  - use ALU, but sign-extend offset
- Load: Read memory and update register
- Store: Write register value to memory

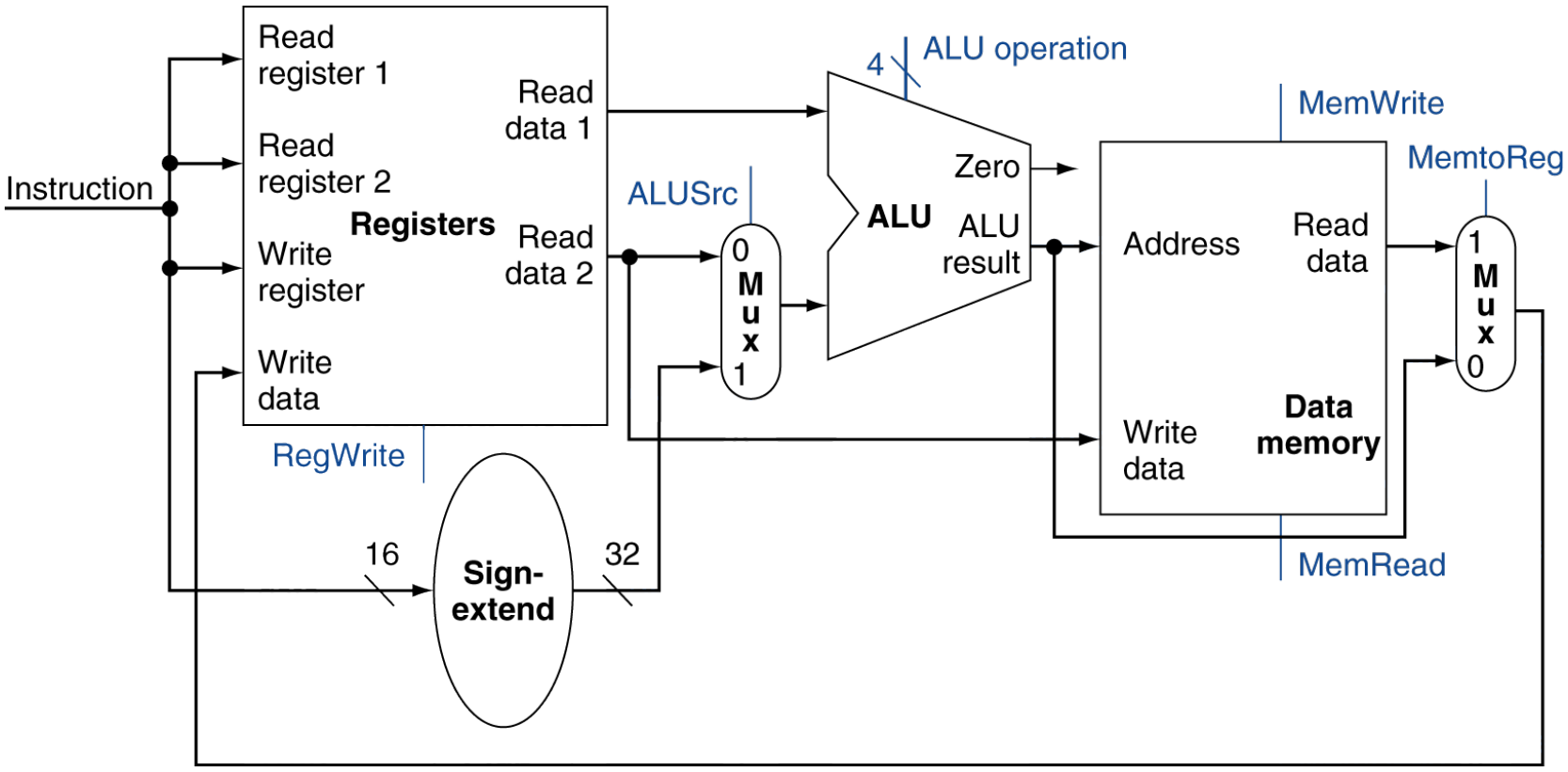


a. Data memory unit



b. Sign extension unit

R-Type/Load/Store Datapath

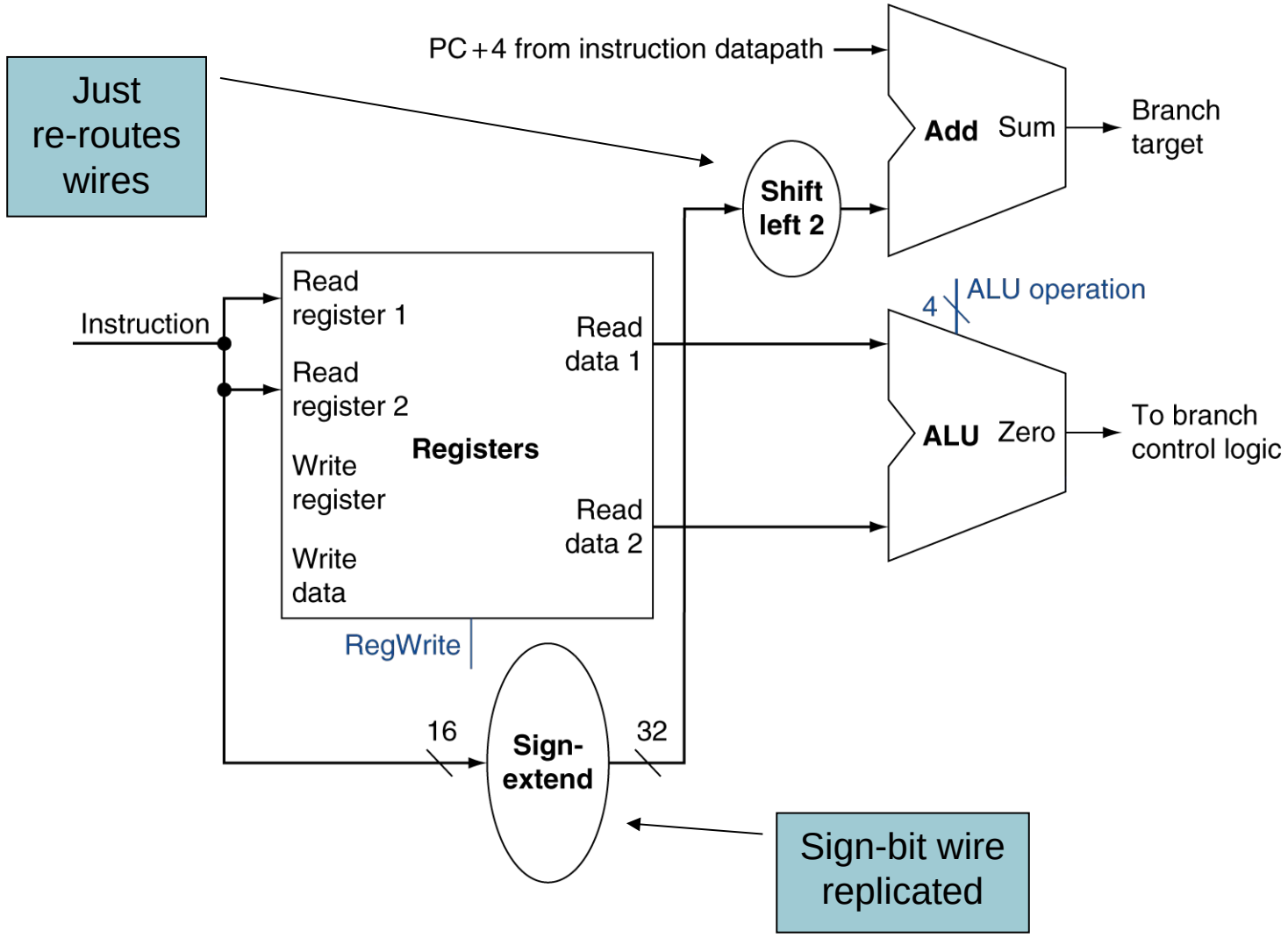


Branch Instructions

Name	Fields						Comments
Field size	6 bits	5 bits	5 bits	5 bits	5 bits	6 bits	All MIPS instructions are 32 bits long
R-format	op	rs	rt	rd	shamt	funct	Arithmetic instruction format
I-format	op	rs	rt	address/immediate			Transfer, branch, imm. format
J-format	op	target address					Jump instruction format

- Read register operands
- Compare operands
  - Use ALU, subtract and check Zero output
- Calculate target address
  - Sign-extend displacement
  - Shift left 2 places
    (instructions are word-aligned)
  - Add to PC **+ 4**
    - Already calculated by instruction fetch

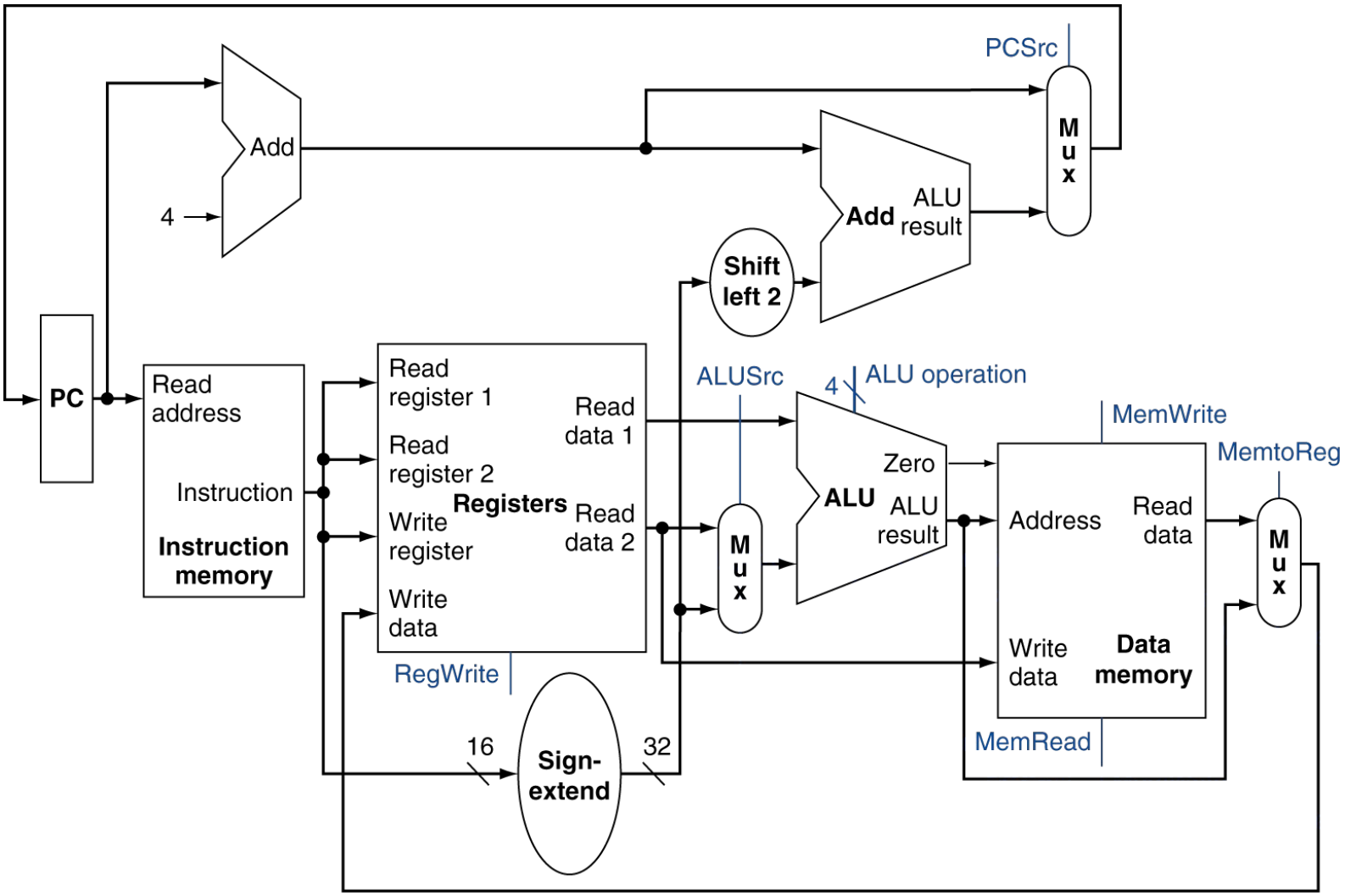
Branch Instructions



Composing the Elements

- First attempt at datapath processes one **instruction** in **one clock cycle**
  - Each datapath element can only do one function at a time (*i.e.,* in one clock cycle)
  - Hence, we need **separate** instruction and data memories!
- Use **multiplexers** where **alternate data sources** (*e.g.,* from ALU or from memory) are used for different instructions

Full Datapath



ALU Control

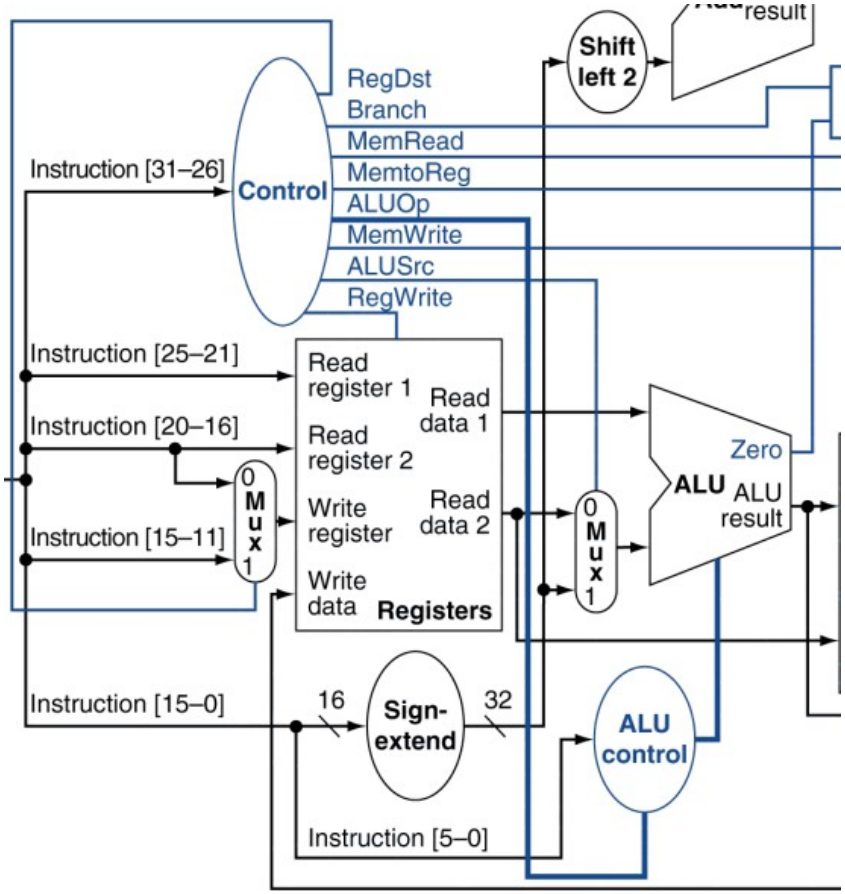
- ALU used for
  - R-type: Function depends on `funct` field
  - Load/Store: Function = **add**
  - Branch `beq`: Function = **subtract**

ALU control	Function
0000	AND
0001	OR
0010	add
0110	subtract
0111	set-on-less-than
1100	NOR

ALU Control

- 2-bit ALUOp derived from opcode

R-type	0	rs	rt	rd	shamt	funct
	31:26	25:21	20:16	15:11	10:6	5:0
Load/ Store	35 or 43	rs	rt	address		
	31:26	25:21	20:16	15:0		
Branch	4	rs	rt	address		
	31:26	25:21	20:16	15:0		



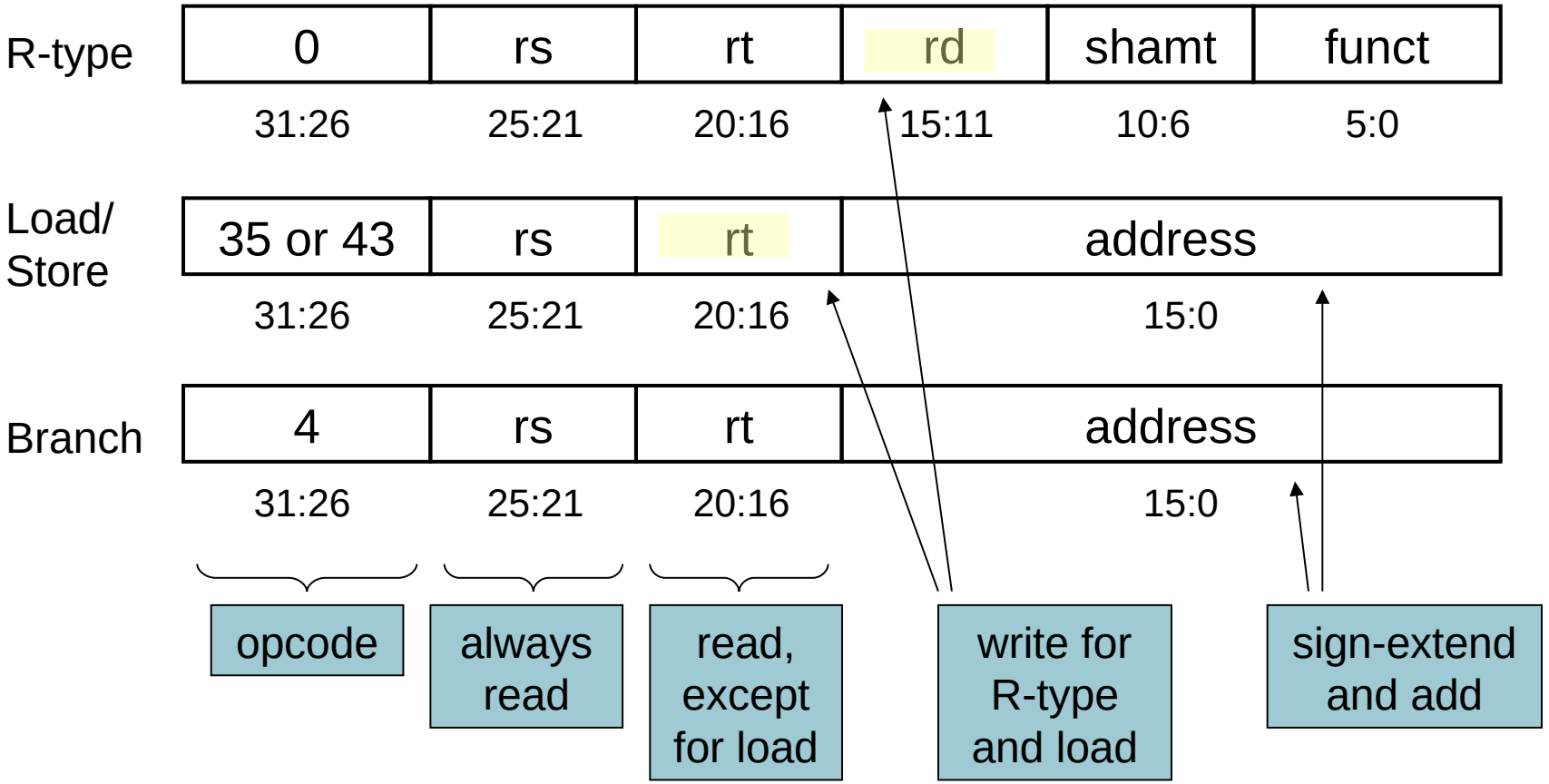
ALU Control

- 2-bit ALUOp derived from opcode
- Combinational logic for ALU control

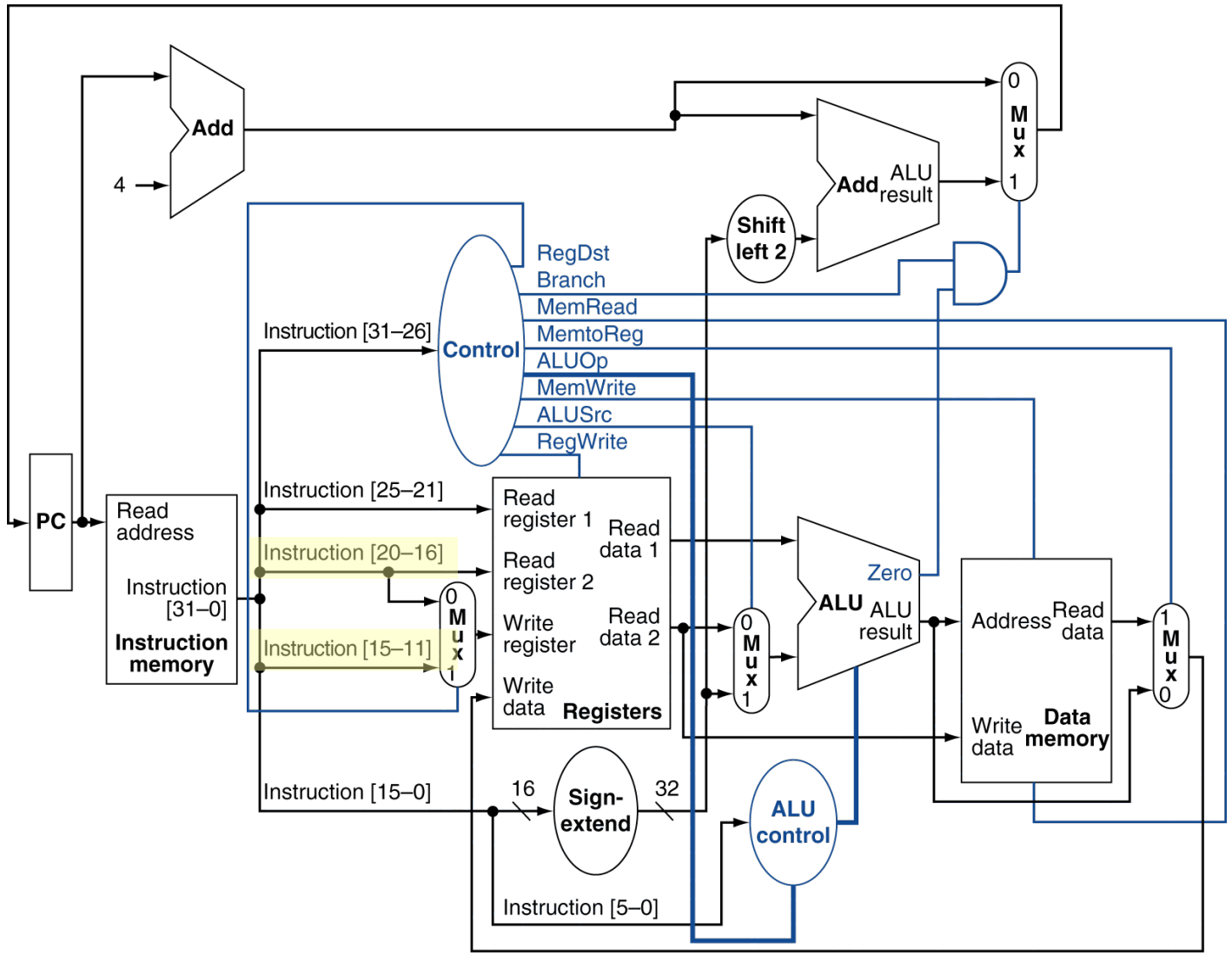
opcode	ALUOp	Operation	funct	ALU function	ALU control
lw	00	load word	XXXXXX	add	0010
sw	00	store word	XXXXXX	add	0010
beq	01	branch equal	XXXXXX	subtract	0110
R-type	10	add	100000	add	0010
		subtract	100010	subtract	0110
		AND	100100	AND	0000
		OR	100101	OR	0001
		set-on-less-than	101010	set-on-less-than	0111

The Main Control Unit

- information extracted from instruction



Datapath With Control



Example program

```
1          .data
2
3  values: .word   10
4          .word   12
5  result: .word   9
6
7          .text
8  start:
9
10 # ALU operations
11         li   $t1, 1
12         li   $t2, 2
13         add  $t3, $t1, $t2
14
15 # memory operations
16         la   $t0, values
17         lw   $t1, 0($t0)
18         lw   $t2, 4($t0)
19         add  $t3, $t1, $t2
20         la   $t0, result
21         sw   $t3, 0($t0)
22
23 # control flow
24         beq  $t3, $t3, start
25         addi $t3, $t3, 2
26
27         j    start
```

Example program, assembled

Text Segment

Bkpt	Address	Code	Basic	Source			
	0x00400000	0x24090001	addiu $9,$0,0x00000001	11:	li	$t1, 1	
	0x00400004	0x240a0002	addiu $10,$0,0x0000...	12:	li	$t2, 2	
	0x00400008	0x012a5820	add $11,$9,$10	13:	add	$t3, $t1, $t2	
	0x0040000c	0x3c011001	lui $1,0x00001001	16:	la	$t0, values	
	0x00400010	0x34280000	ori $8,$1,0x00000000				
	0x00400014	0x8d090000	lw $9,0x00000000($8)	17:	lw	$t1, 0($t0)	
	0x00400018	0x8d0a0004	lw $10,0x00000004($8)	18:	lw	$t2, 4($t0)	
	0x0040001c	0x012a5820	add $11,$9,$10	19:	add	$t3, $t1, $t2	
	0x00400020	0x3c011001	lui $1,0x00001001	20:	la	$t0, result	
	0x00400024	0x34280008	ori $8,$1,0x00000008				
	0x00400028	0xad0b0000	sw $11,0x00000000($8)	21:	sw	$t3, 0($t0)	
	0x0040002c	0x116bfff4	beq $11,$11,0xfffffff4	24:	beq	$t3, $t3, start	
	0x00400030	0x216b0002	addi $11,$11,0x0000...	25:	addi	$t3, $t3, 2	
	0x00400034	0x08100000	j 0x00400000	27:	j	start	

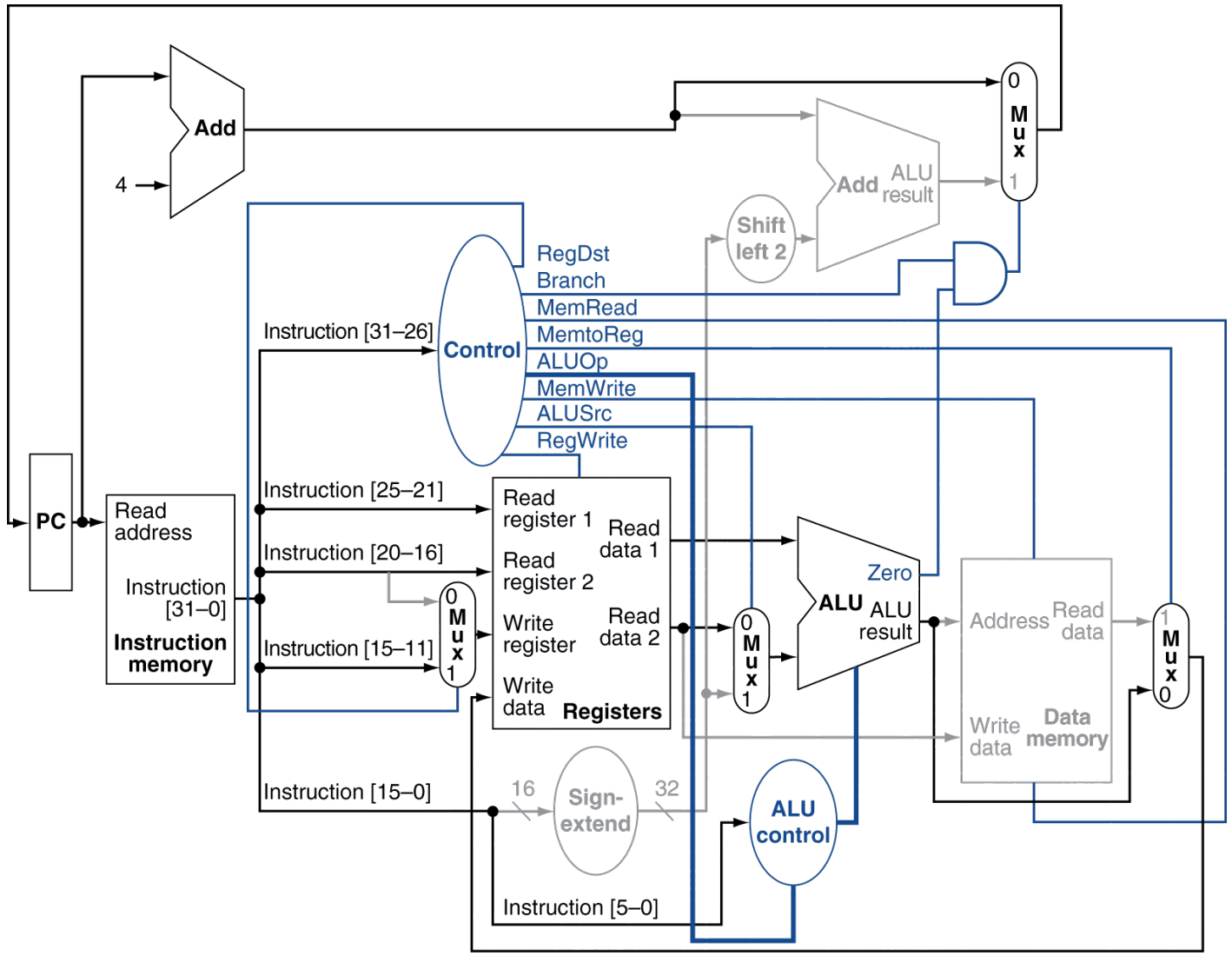
Labels

Label	Address ▲
tst.asm	
start	0x00400000
values	0x10010000
result	0x10010008

Data Segment

Address	Value (+0)	Value (+4)	Value (+8)	Value (+c)	Value (+10)	Value (+14)	Value (+18)	
0x10010000	0x0000000a	0x0000000c	0x00000009	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010020	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010040	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010060	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010080	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x100100a0	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x100100c0	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x100100e0	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010100	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010120	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010140	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010160	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x10010180	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x100101a0	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x100101c0	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000
0x100101e0	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000	0x00000000

R-Type Instruction




```
0x0040001c  0x012a5820  add $11,$9,$10        19:          add  $t3, $t1, $t2
```

R-Type Instruction encoding

0x0040001c	0x012a5820	add $11,$9,$10	19:	add $t3, $t1, $t2

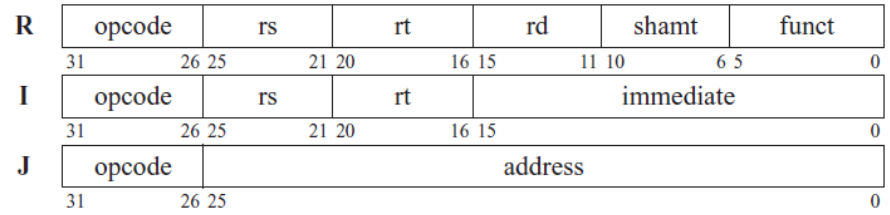
MIPS Reference Data

CORE INSTRUCTION SET

NAME, MNEMONIC		FOR-MAT	OPERATION (in Verilog)		OPCODE / FUNCT (Hex)
Add	add	R	R[rd] = R[rs] + R[rt]	(1)	$0 / 20_{hex}$
Add Immediate	addi	I	R[rt] = R[rs] + SignExtImm	(1,2)	8_{hex}
Add Imm. Unsigned	addiu	I	R[rt] = R[rs] + SignExtImm	(2)	9_{hex}
Add Unsigned	addu	R	R[rd] = R[rs] + R[rt]		$0 / 21_{hex}$
And	and	R	R[rd] = R[rs] & R[rt]		$0 / 24_{hex}$
And Immediate	andi	I	R[rt] = R[rs] & ZeroExtImm	(3)	c_{hex}
Branch On Equal	beq	I	if(R[rs]==R[rt]) PC=PC+4+BranchAddr	(4)	4_{hex}

(1) May cause overflow exception
(2) SignExtImm = { 16{immediate[15]}, immediate }
(3) ZeroExtImm = { 16{1b'0}, immediate }
(4) BranchAddr = { 14{immediate[15]}, immediate, 2'b0 }
(5) JumpAddr = { PC+4[31:28], address, 2'b0 }
(6) Operands considered unsigned numbers (vs. 2's comp.)
(7) Atomic test&set pair; R[rt] = 1 if pair atomic, 0 if not atomic

BASIC INSTRUCTION FORMATS



add opcode = 00_{16} = 000000_2
add func = 20_{16} = 100000_2
add shamt = 00_{16} = 00000_2
$t1 = $9 = 01001_2
$t2 = $10 = 01010_2
$t3 = $11 = 01011_2

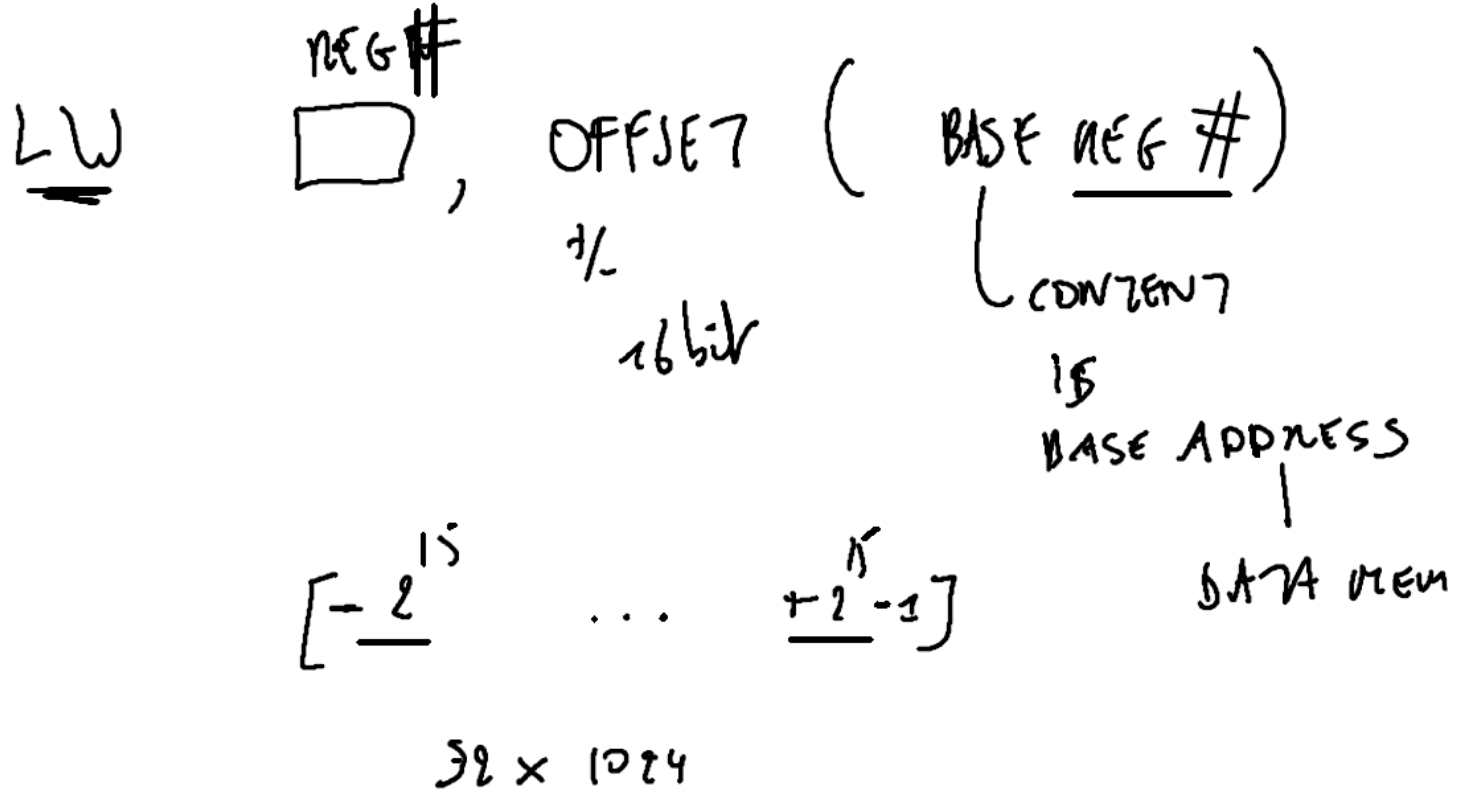
encoding of add $t3, $t1, $t2

= 000000 01001 01010 01011 00000 100000_2

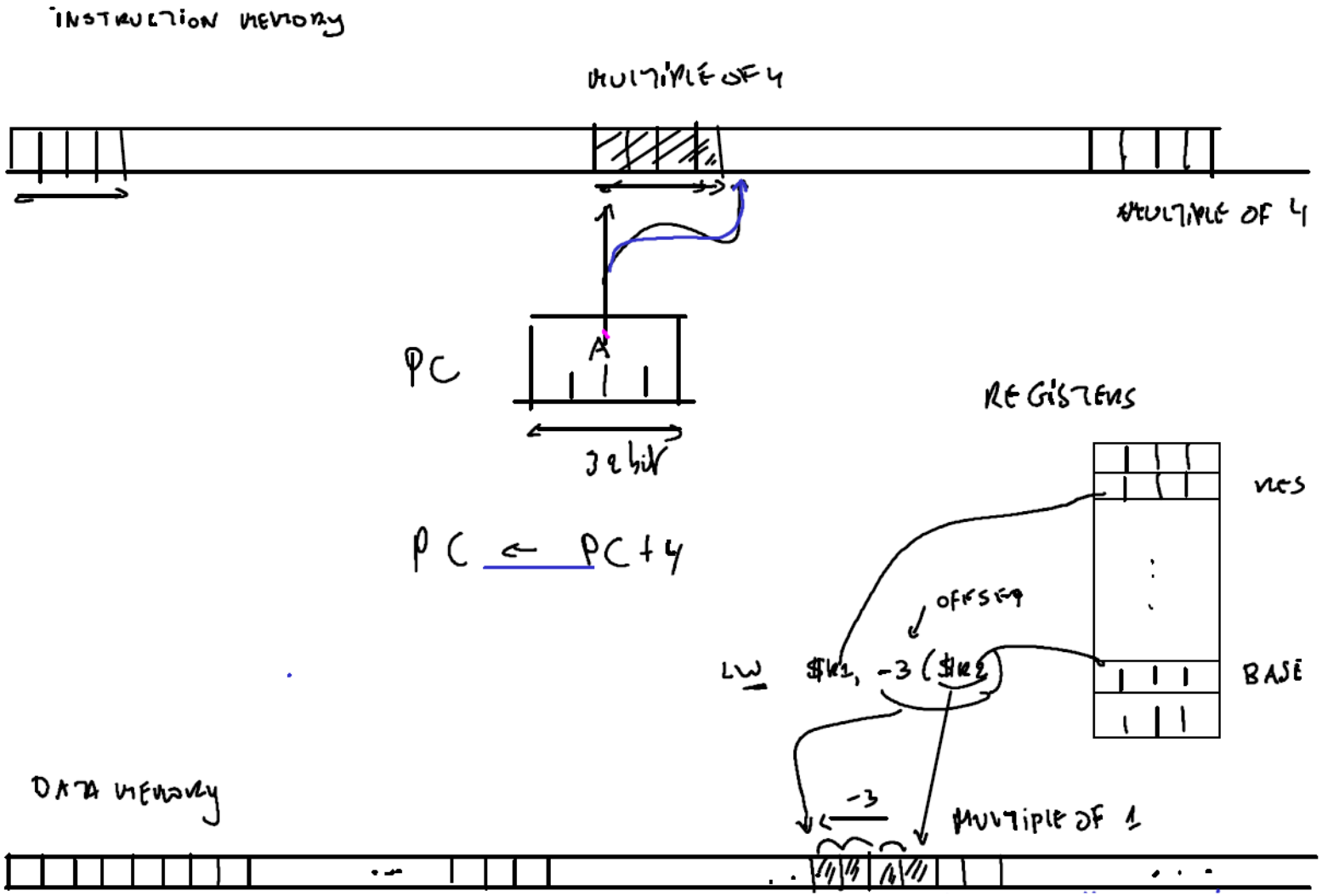
= 0000 0001 0010 1010 0101 1000 0010 0000_2

= 0 1 2 a 5 8 2 0_{16}

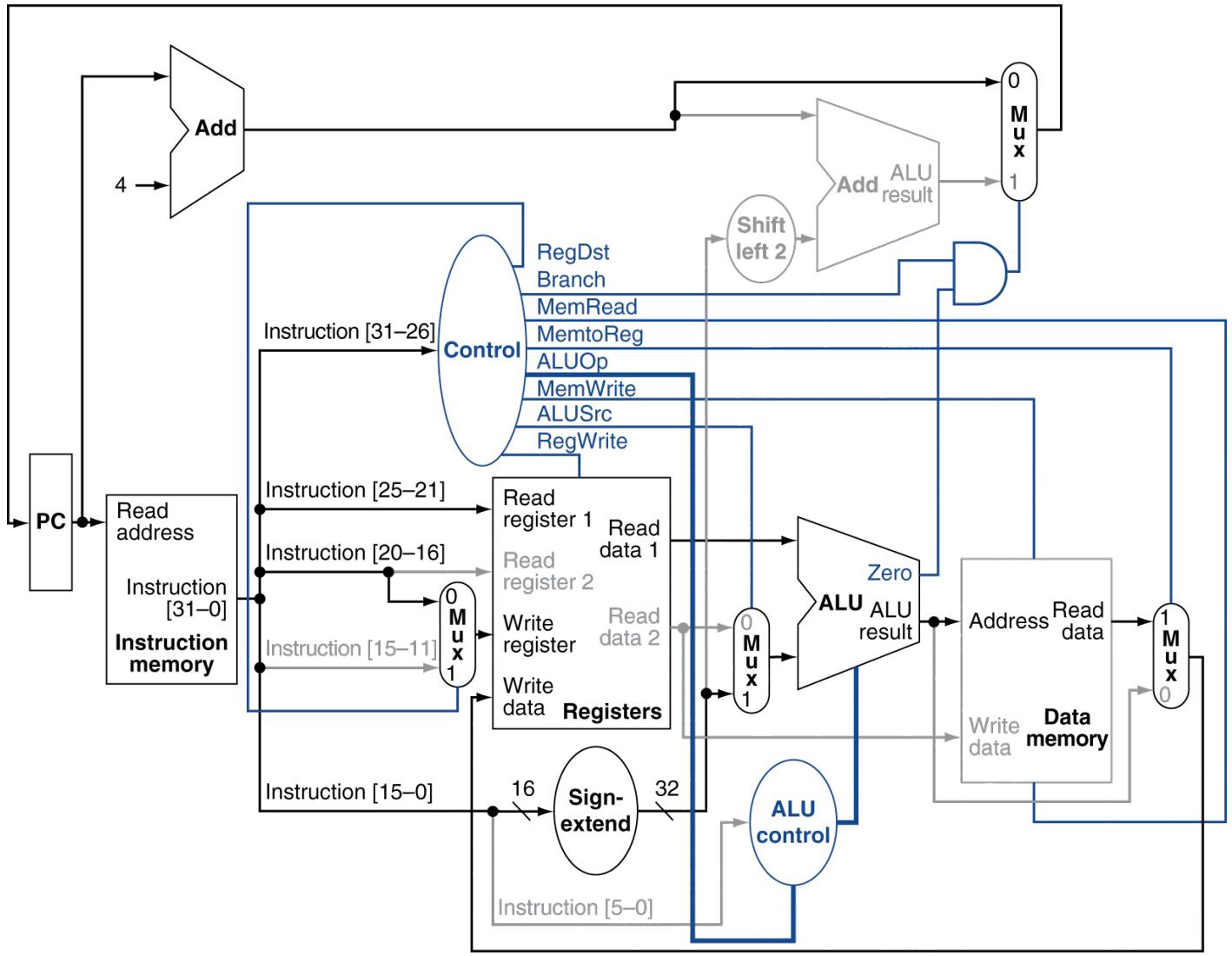
Load Instruction



Load Instruction



Load Instruction



0x00400018 | 0x8d0a0004 | lw $10,0x00000004($8) | 18: lw $t2, 4($t0)

Load Instruction encoding

```
0x00400018  0x8d0a0004  lw $10,0x00000004($8)  18:          lw   $t2, 4($t0)
```

MIPS Reference Data

CORE INSTRUCTION SET

NAME, MNEMONIC		FOR-MAT	OPERATION (in Verilog)		OPCODE / FUNCT (Hex)
Add	add	R	R[rd] = R[rs] + R[rt]	(1)	0 / 20_{hex}
Add Immediate	addi	I	R[rt] = R[rs] + SignExtImm	(1,2)	8_{hex}
Add Imm. Unsigned	addiu	I	R[rt] = R[rs] + SignExtImm	(2)	9_{hex}
Add Unsigned	addu	R	R[rd] = R[rs] + R[rt]		0 / 21_{hex}
And	and	R	R[rd] = R[rs] & R[rt]		0 / 24_{hex}
And Immediate	andi	I	R[rt] = R[rs] & ZeroExtImm	(3)	c_{hex}
Branch On Equal	beq	I	if(R[rs]==R[rt]) PC=PC+4+BranchAddr	(4)	4_{hex}
Branch On Not Equal	bne	I	if(R[rs]!=R[rt]) PC=PC+4+BranchAddr	(4)	5_{hex}
Jump	j	J	PC=JumpAddr	(5)	2_{hex}
Jump And Link	jal	J	R[31]=PC+8;PC=JumpAddr	(5)	3_{hex}
Jump Register	jr	R	PC=R[rs]		0 / 08_{hex}
Load Byte Unsigned	lbu	I	R[rt]={24'b0,M[R[rs] +SignExtImm](7:0)}	(2)	24_{hex}
Load Halfword Unsigned	lhu	I	R[rt]={16'b0,M[R[rs] +SignExtImm](15:0)}	(2)	25_{hex}
Load Linked	ll	I	R[rt] = M[R[rs]+SignExtImm]	(2,7)	30_{hex}
Load Upper Imm.	lui	I	R[rt] = {imm, 16'b0}		f_{hex}
Load Word	lw	I	R[rt] = M[R[rs]+SignExtImm]	(2)	23_{hex}

(1) May cause overflow exception
(2) SignExtImm = { 16{immediate[15]}, immediate }
(3) ZeroExtImm = { 16{1b'0}, immediate }
(4) BranchAddr = { 14{immediate[15]}, immediate, 2'b0 }
(5) JumpAddr = { PC+4[31:28], address, 2'b0 }
(6) Operands considered unsigned numbers (vs. 2's comp.)
(7) Atomic test&set pair; R[rt] = 1 if pair atomic, 0 if not atomic

lw opcode = 23_{16} = 100011_2
$t0 = $8 = 01000_2
$t2 = $10 = 01010_2
4 = 0000 0000 0000 0100_2

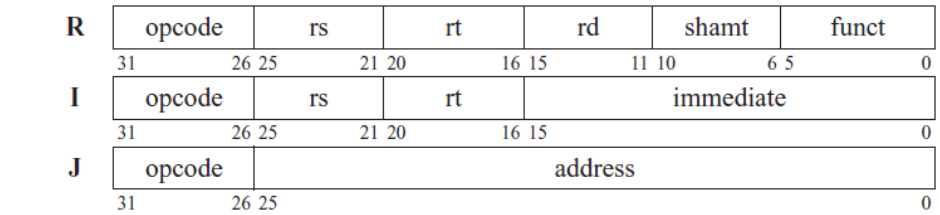
encoding of lw $t2, 4($t0)

= 100011 01000 01010 0000 0000 0000 0100_2

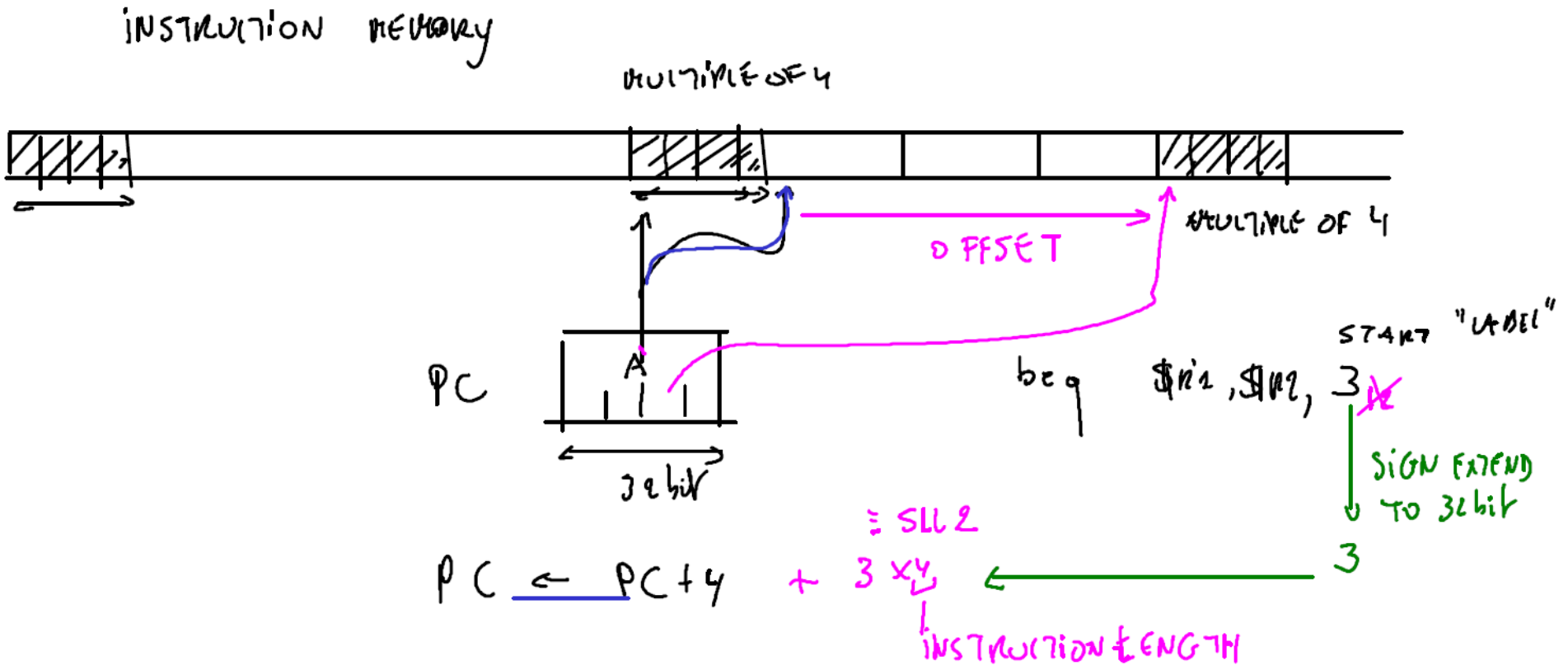
= 1000 1101 0000 1010 0000 0000 0000 0100_2

= 8 d 0 a 0 0 0 4_{16}

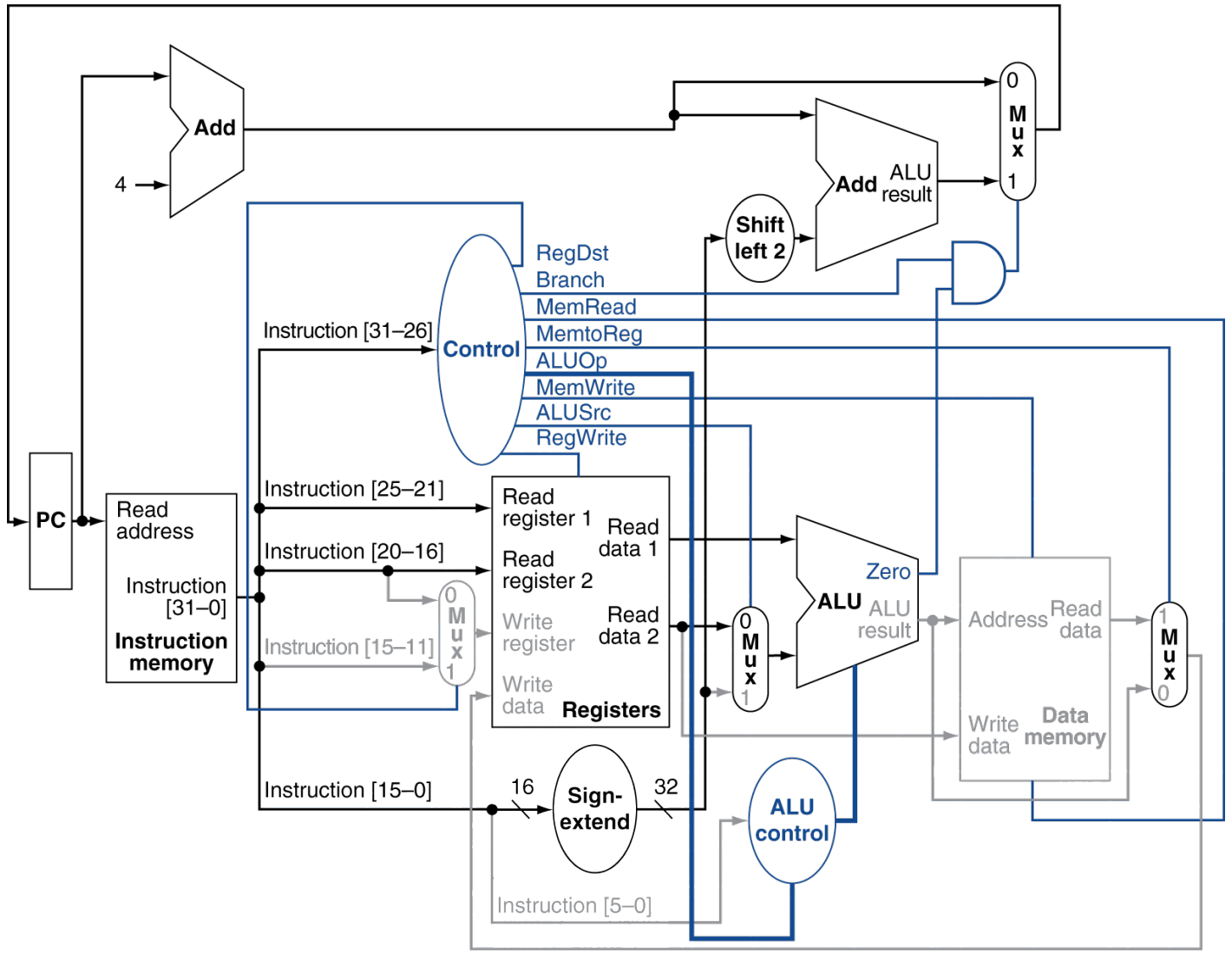
BASIC INSTRUCTION FORMATS



Branch-on-Equal Instruction



Branch-on-Equal Instruction




```
0x0040002c  0x116bfff4  beq $11,$11,0xfffffff4  24:          beq  $t3, $t3, start
```

beq Instruction encoding

0x0040002c	0x116bfff4	beq $11,$11,0xfffffff4	24:	beq $t3, $t3, start

Text Segment

Bkpt	Address	Code	Basic	Source
	0x00400000	0x24090001	addiu $9,$0,0x00000001	11: li $t1, 1
	0x00400004	0x240a0002	addiu $10,$0,0x0000...	12: li $t2, 2
	0x00400008	0x012a5820	add $11,$9,$10	13: add $t3, $t1, $t2
	0x0040000c	0x3c011001	lui $1,0x00001001	16: la $t0, values
	0x00400010	0x34280000	ori $8,$1,0x00000000	
	0x00400014	0x8d090000	lw $9,0x00000000($8)	17: lw $t1, 0($t0)
	0x00400018	0x8d0a0004	lw $10,0x00000004($8)	18: lw $t2, 4($t0)
	0x0040001c	0x012a5820	add $11,$9,$10	19: add $t3, $t1, $t2
	0x00400020	0x3c011001	lui $1,0x00001001	20: la $t0, result
	0x00400024	0x34280008	ori $8,$1,0x00000008	
	0x00400028	0xad0b0000	sw $11,0x00000000($8)	21: sw $t3, 0($t0)
→	0x0040002c	0x116bfff4	beq $11,$11,0xfffffff4	24: beq $t3, $t3, start
	0x00400030	0x216b0002	addi $11,$11,0x0000...	25: addi $t3, $t3, 2
	0x00400034	0x08100000	j 0x00400000	27: j start

```
        .text
start:

# ALU operations
        li   $t1, 1
        li   $t2, 2
        add  $t3, $t1, $t2
```

start = PC + 4 + offset (in words)

→ offset = -12_{10}

12_{10} = 0000 0000 0000 1100$_2$

-12_{10} = 1111 1111 1111 0011$_2$

+ 0000 0000 0000 0001$_2$

= 1111 1111 1111 0100$_2$

= FFF4$_{16}$

beq Instruction encoding

0x0040002c	0x116bfff4	beq $11,$11,0xfffffff4	24:	beq $t3, $t3, start

MIPS Reference Data

CORE INSTRUCTION SET

NAME, MNEMONIC		FOR-MAT	OPERATION (in Verilog)		OPCODE / FUNCT (Hex)
Add	add	R	R[rd] = R[rs] + R[rt]	(1)	$0 / 20_{hex}$
Add Immediate	addi	I	R[rt] = R[rs] + SignExtImm	(1,2)	8_{hex}
Add Imm. Unsigned	addiu	I	R[rt] = R[rs] + SignExtImm	(2)	9_{hex}
Add Unsigned	addu	R	R[rd] = R[rs] + R[rt]		$0 / 21_{hex}$
And	and	R	R[rd] = R[rs] & R[rt]		$0 / 24_{hex}$
And Immediate	andi	I	R[rt] = R[rs] & ZeroExtImm	(3)	c_{hex}
Branch On Equal	beq	I	if(R[rs]==R[rt]) PC=PC+4+BranchAddr	(4)	4_{hex}
Branch On Not Equal	bne	I	if(R[rs]!=R[rt]) PC=PC+4+BranchAddr	(4)	5_{hex}

(1) May cause overflow exception
(2) SignExtImm = { 16{immediate[15]}, immediate }
(3) ZeroExtImm = { 16{1b'0}, immediate }
(4) BranchAddr = { 14{immediate[15]}, immediate, 2'b0 }
(5) JumpAddr = { PC+4[31:28], address, 2'b0 }
(6) Operands considered unsigned numbers (vs. 2's comp.)
(7) Atomic test&set pair; R[rt] = 1 if pair atomic, 0 if not atomic

beq opcode = 4_{16} = 000100_2
$t3 = $11 = 01011_2
offset = $FFF4_{16}$ = $1111\ 1111\ 1111\ 0100_2$

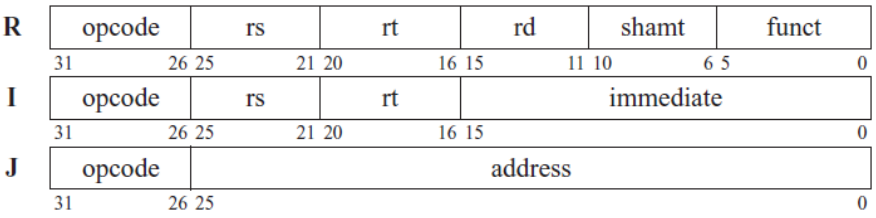
encoding of beq $t3, $t3, start

= $000100\ 01011\ 01011\ 1111\ 1111\ 1111\ 0100_2$

= $0001\ 0001\ 0110\ 1011\ 1111\ 1111\ 1111\ 0100_2$

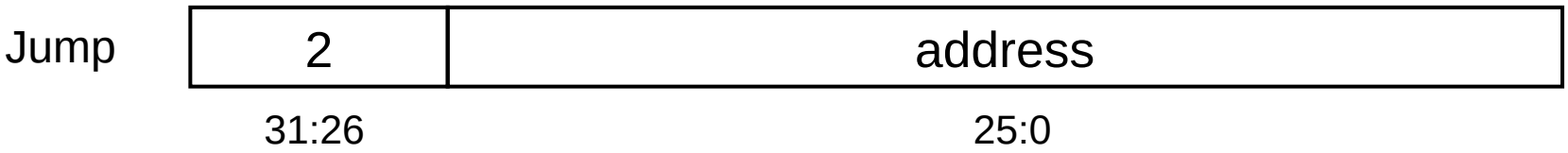
= $1\ 1\ 6\ b\ f\ f\ f\ 4_{16}$

BASIC INSTRUCTION FORMATS



Implementing Jumps

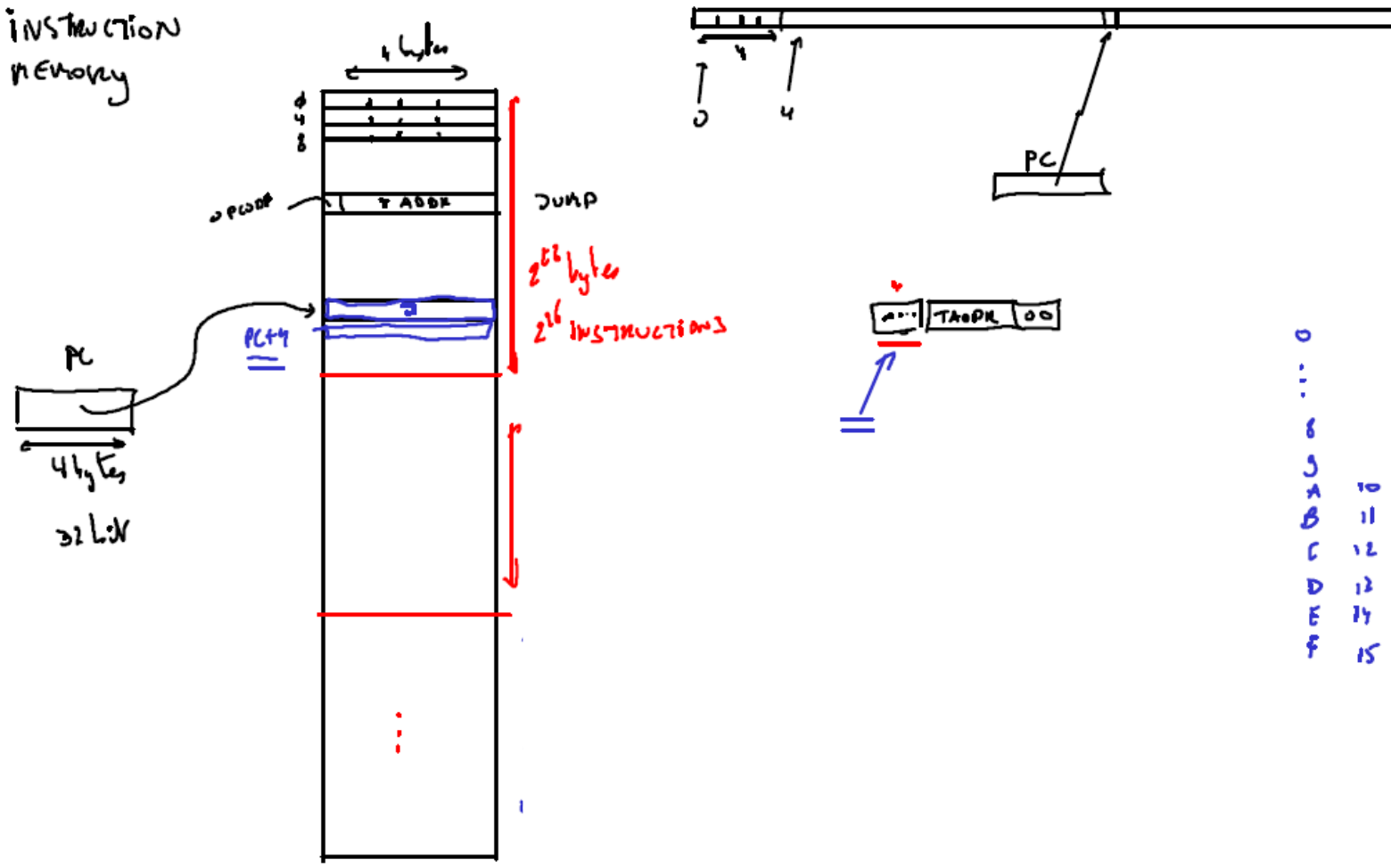
Name	Fields						Comments
Field size	6 bits	5 bits	5 bits	5 bits	5 bits	6 bits	All MIPS instructions are 32 bits long
R-format	op	rs	rt	rd	shamt	funct	Arithmetic instruction format
I-format	op	rs	rt	address/immediate			Transfer, branch, imm. format
J-format	op	target address					Jump instruction format



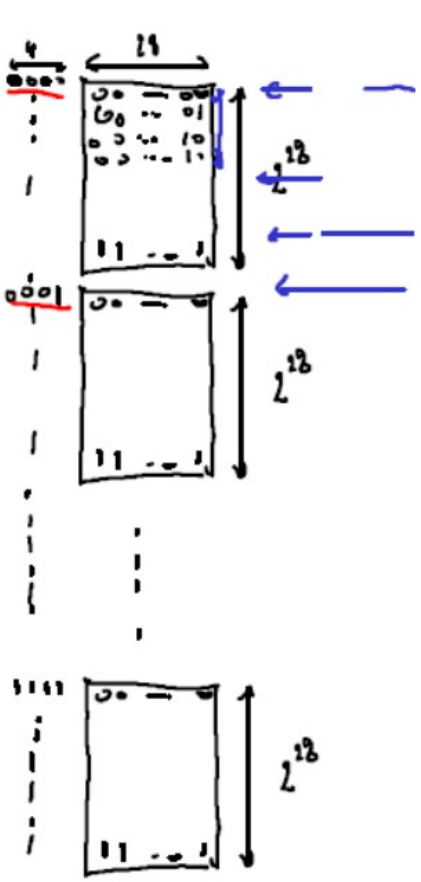
- Jump uses **word** address (not byte address)
- Update (32 bit) PC with concatenation of
  - **top 4 bits** of (**old PC + 4**)
  - 26-bit jump address
  - 00
- Need extra control signal (for PC mux): decoded from opcode

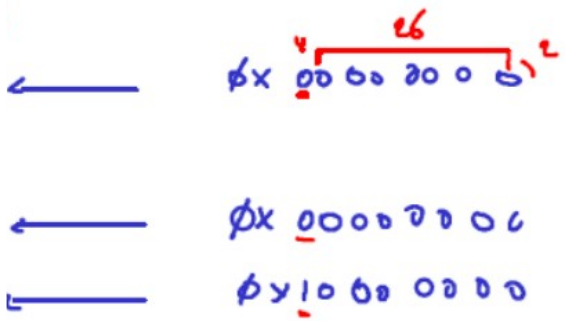
0x00400034	0x08100000	j 0x00400000	27:	j start

Implementing Jumps



Implementing Jumps





jump Instruction encoding

0x00400034	0x08100000	j 0x00400000	27:	j	start

MIPS Reference Data

CORE INSTRUCTION SET

NAME, MNEMONIC		FOR-MAT	OPERATION (in Verilog)		OPCODE / FUNCT (Hex)
Add	add	R	R[rd] = R[rs] + R[rt]	(1)	$0 / 20_{hex}$
Add Immediate	addi	I	R[rt] = R[rs] + SignExtImm	(1,2)	8_{hex}
Add Imm. Unsigned	addiu	I	R[rt] = R[rs] + SignExtImm	(2)	9_{hex}
Add Unsigned	addu	R	R[rd] = R[rs] + R[rt]		$0 / 21_{hex}$
And	and	R	R[rd] = R[rs] & R[rt]		$0 / 24_{hex}$
And Immediate	andi	I	R[rt] = R[rs] & ZeroExtImm	(3)	c_{hex}
Branch On Equal	beq	I	if(R[rs]==R[rt]) PC=PC+4+BranchAddr	(4)	4_{hex}
Branch On Not Equal	bne	I	if(R[rs]!=R[rt]) PC=PC+4+BranchAddr	(4)	5_{hex}
Jump	j	J	PC=JumpAddr	(5)	2_{hex}

(1) May cause overflow exception
(2) SignExtImm = { 16{immediate[15]}, immediate }
(3) ZeroExtImm = { 16{1b'0}, immediate }
(4) BranchAddr = { 14{immediate[15]}, immediate, 2'b0 }
(5) JumpAddr = { PC+4[31:28], address, 2'b0 }
(6) Operands considered unsigned numbers (vs. 2's comp.)
(7) Atomic test&set pair; R[rt] = 1 if pair atomic, 0 if not atomic

j opcode = 2_{16} = 000010_2

PC = 004000034_{16}

PC + 4 = 004000038_{16}

top 4 bits of (PC + 4) = 0_{16} = 0000_2

target address
= 00400000_{16}
= 0000 **0000 0100 0000 0000 0000 0000 00**00_2
26 bit address

encoding of j start

= 000010 0000 0100 0000 0000 0000 0000 00_2

= 0000 1000 0001 0000 0000 0000 0000 0000_2

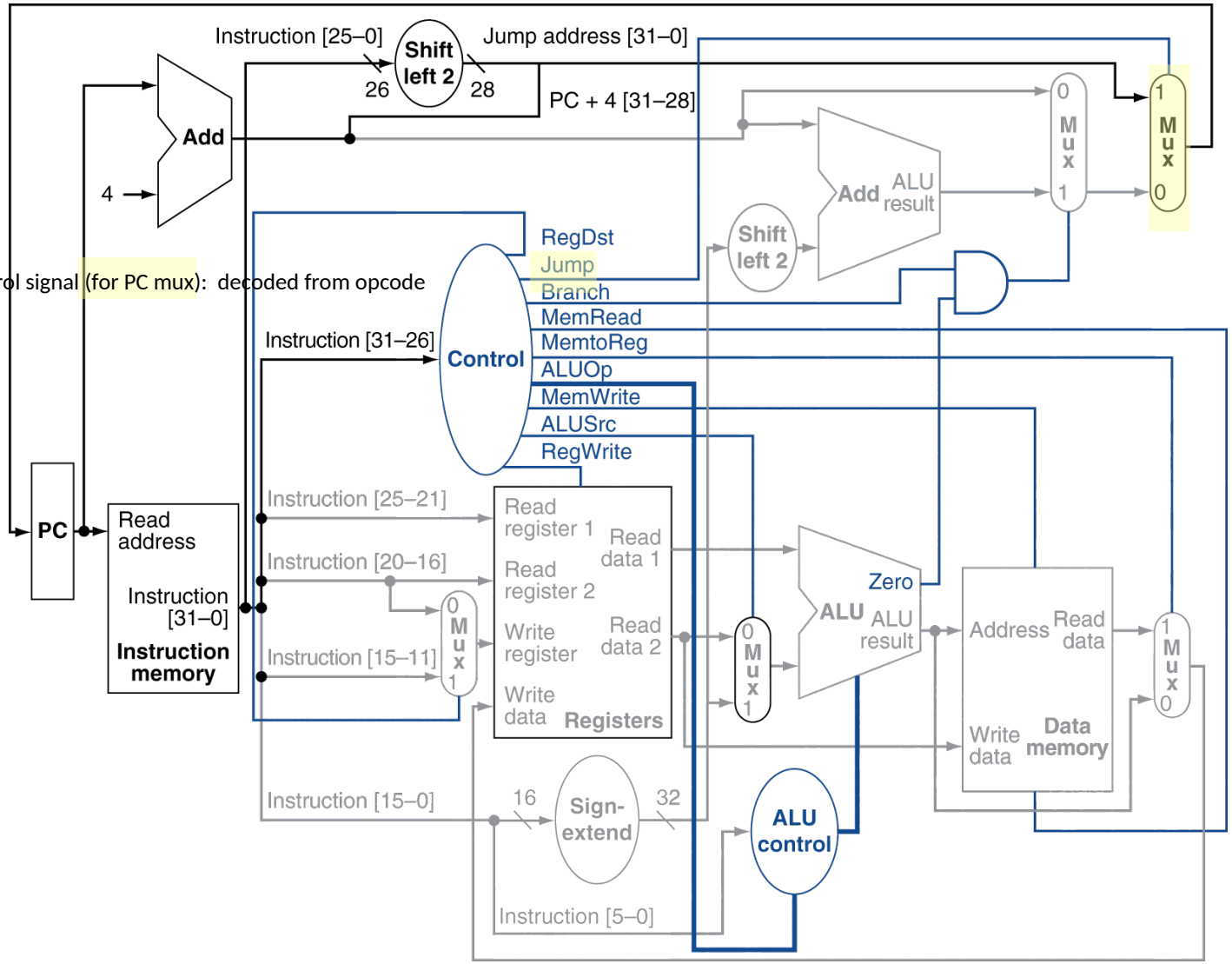
= 0 8 1 0 0 0 0 0_{16}

start:

Text Segment

Bkpt	Address	Code	Basic		Source	
	0x00400000	0x24090001	addiu $9,$0,0x00000001	11:	li	$t1, 1
	0x00400004	0x240a0002	addiu $10,$0,0x0000...	12:	li	$t2, 2
	0x00400008	0x012a5820	add $11,$9,$10	13:	add	$t3, $t1, $t2
	0x0040000c	0x3c011001	lui $1,0x00001001	16:	la	$t0, values
	0x00400010	0x34280000	ori $8,$1,0x00000000			
	0x00400014	0x8d090000	lw $9,0x00000000($8)	17:	lw	$t1, 0($t0)
	0x00400018	0x8d0a0004	lw $10,0x00000004($8)	18:	lw	$t2, 4($t0)
	0x0040001c	0x012a5820	add $11,$9,$10	19:	add	$t3, $t1, $t2
	0x00400020	0x3c011001	lui $1,0x00001001	20:	la	$t0, result
	0x00400024	0x34280008	ori $8,$1,0x00000008			
	0x00400028	0xad0b0000	sw $11,0x00000000($8)	21:	sw	$t3, 0($t0)
	0x0040002c	0x116bfff4	beq $11,$11,0xfffffff4	24:	beq	$t3, $t3, start
	0x00400030	0x216b0002	addi $11,$11,0x0000...	25:	addi	$t3, $t3, 2
	0x00400034	0x08100000	j 0x00400000	27:	j	start

Datapath With Jumps Added



Need extra control signal (for PC mux): decoded from opcode

```
0x00400034  0x08100000  j 0x00400000          27:          j    start
```

Performance Issues

- **Longest delay** determines **clock period**
  - **Critical** path: **load** instruction
  - Instruction memory → register file → ALU → data memory → register file
- Varying clock period for different instructions violates design principles:
  - **regularity**
  - **make the common case fast**
- Will improve performance by Instruction-Level Parallellism (ILP) aka “pipelining”
  (note that a constant clock period is needed for ILP)