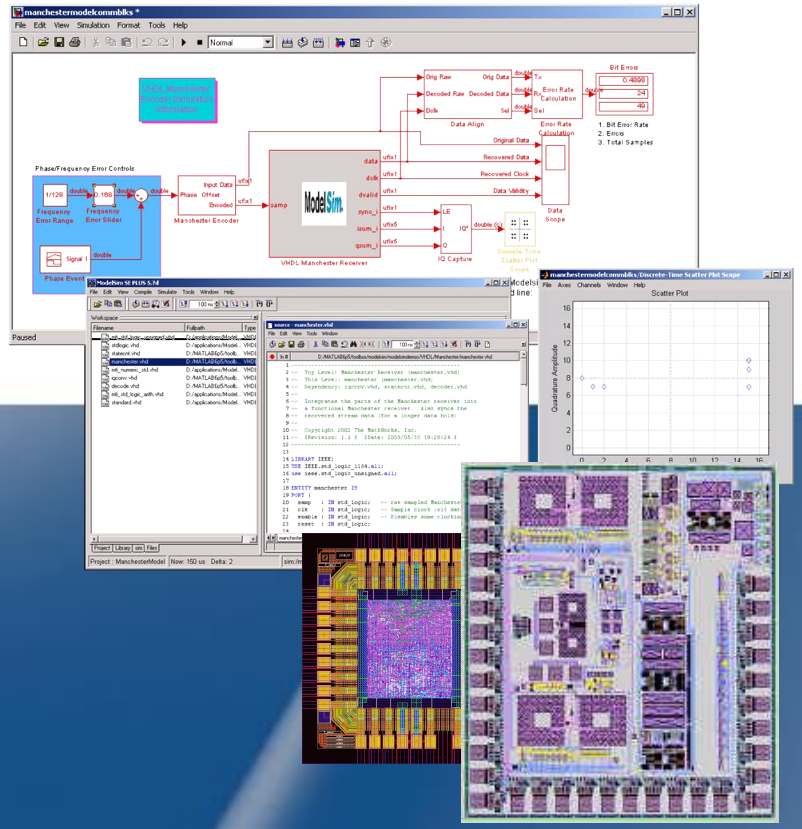
# Model-Based Embedded System Design



Pieter J. Mosterman

Senior Research Scientist
The MathWorks, Inc.

# Agenda

- Introduction
- Embedded Systems Design
- Demo
- A Design Activity
  - Dynamic Voltage Scaling
- Summary

# What is the problem?

- "Hardware verification is itself become more challenging. Verification times have increased with rising gate count and as overall design complexity grows. According to a survey by Collett International Research in 2002 only 39% of designs were bug free at first silicon, while 60% contained logic or functional flaws. More than 20% required 3 or more silicon spins. A Collett survey also showed that nearly 50% of total engineering time was spent in verification."

- Hardware/Software Co-verification by Dr. Jack Horgan http://www.edacafe.com/magazine/index.php?newsletter=1&run_date=29-Mar-2004

# What are the pains?

1. Time and effort to verify a design: As designs get more complex, the test benches are an order of magnitude more complex, and consume 40-60% of project resources.
   - Test bench HDL code will *not* be synthesized – i.e., will not be a part of the shipping product – "throw-away" code
   - HDL test benches need to run in HDL simulators, and HDL simulators are *extremely* slow

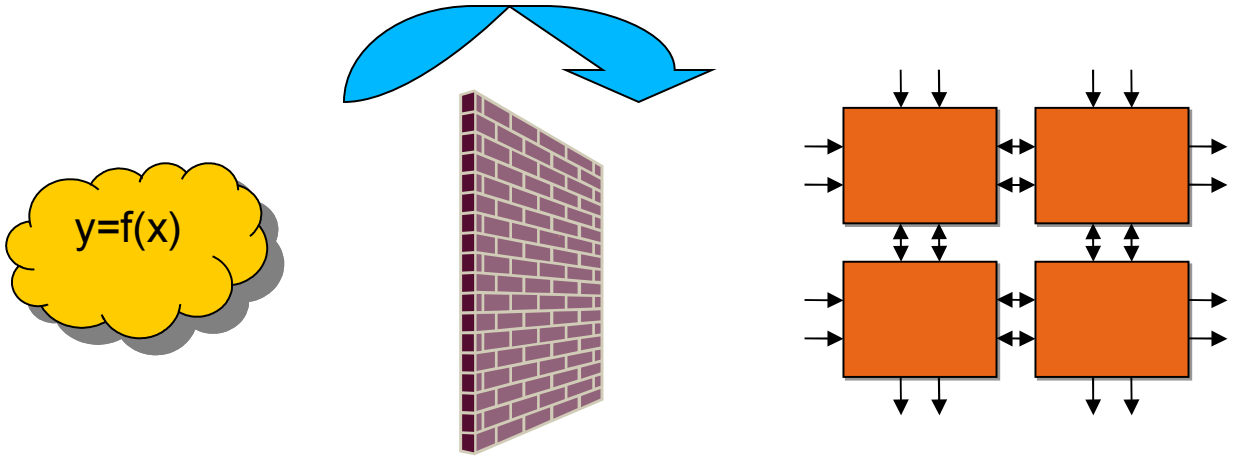
2. Time and effort to construct and maintain test benches: For each line of HDL design code in a design, a user typically needs 10 lines of HDL test bench code to simulate, test, and verify that 1 line of HDL code.
   - Constructing a test bench in a textual language is at least as complex as the original design itself
   - Maintaining the test bench from one generation of a design to the next is very resource-intensive

# Agenda

- Introduction
- **Embedded Systems Design**
- Demo
- Mixed Signal Simulation
- Summary

# What are the pains?

- **Engineers need to verify that ASIC/FPGA implementations correctly match their system specifications**

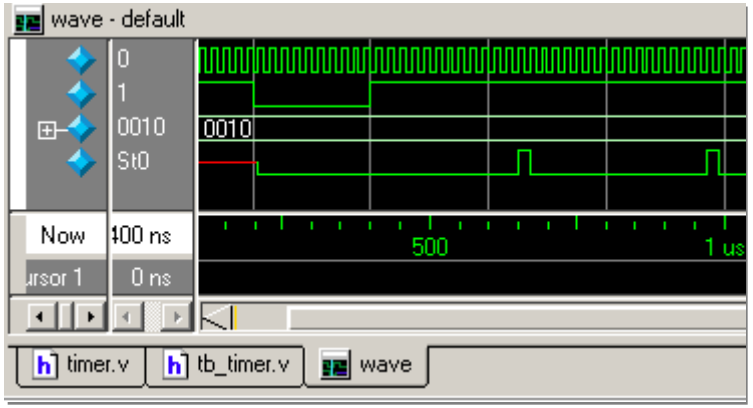



I/O vectors,
functional specification

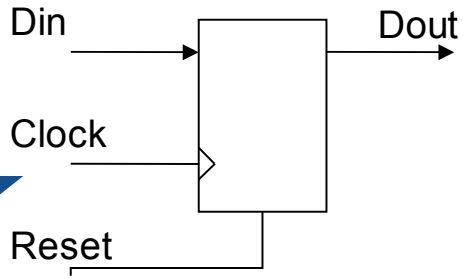
# ASIC/FPGA design flow beings in HDL

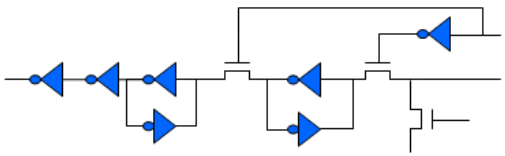
```
1   //Verilog Model of a D Flip Flop
2   module flipflop (dout, din, clock, reset);
3   output dout;
4   input din, clock, reset;
5
6   reg dout;
7
8   always @(posedge clock)
9   begin
10      if (reset)
11      dout <= 1'b0;
12      else
13      dout <= din;
14  end
15  endmodule //flipflop
```

Simulate RTL

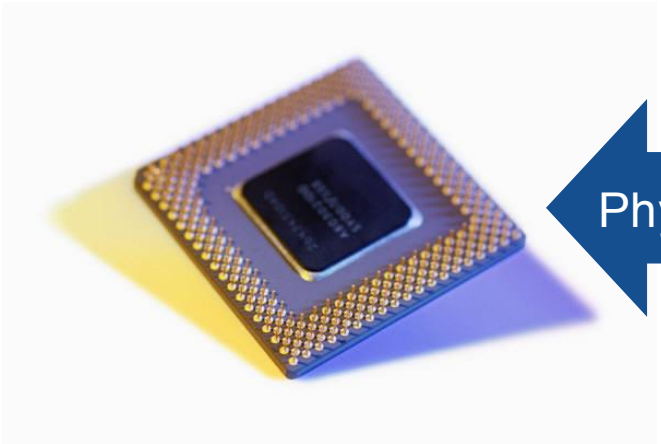



Synthesis



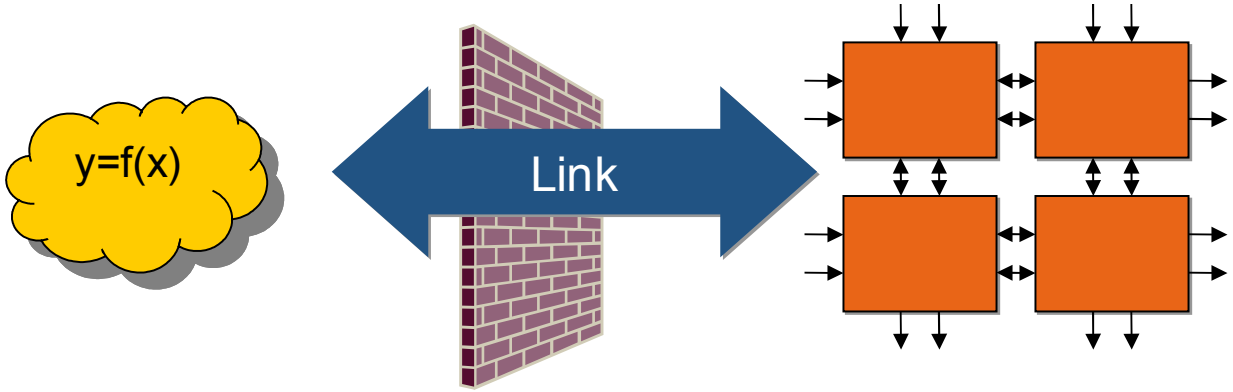



Physical Design



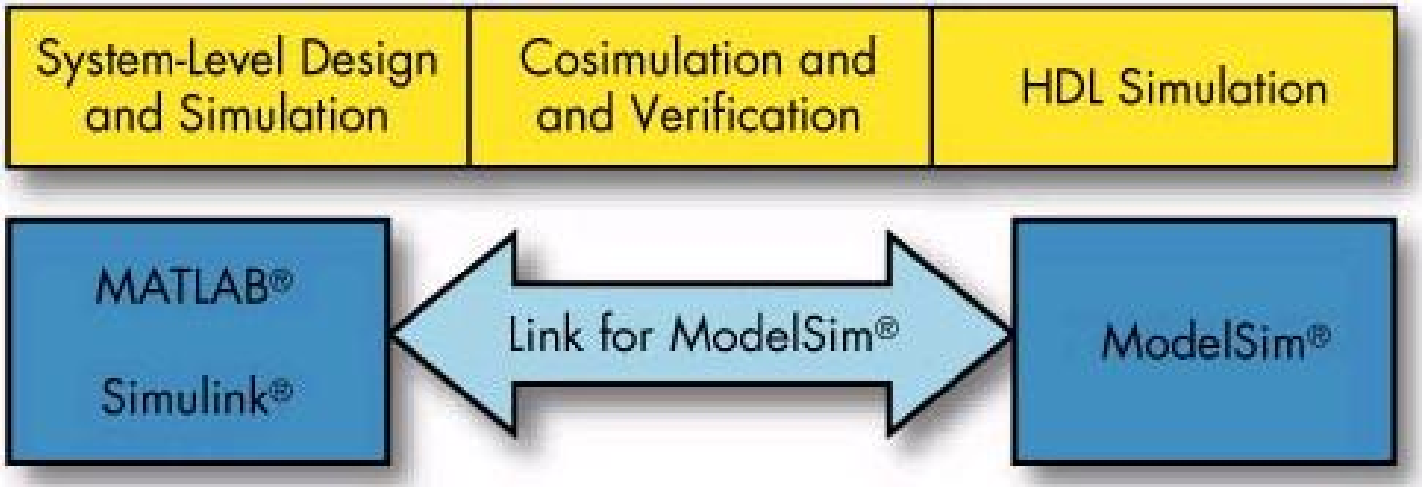
# What are the solutions?

- **Engineers need to verify that ASIC/FPGA implementations correctly match their system specifications**




- **Using co-simulation with a cycle accurate simulator, these engineers can analyze hardware components at a system level**

# Link for ModelSim makes system-level hardware verification possible



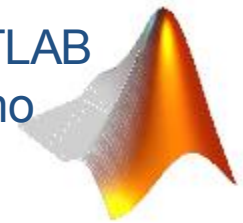

- **Fast and bidirectional cosimulation interface between MATLAB and Simulink, and ModelSim**

# Agenda

- Introduction
- Embedded Systems Design
- **Demo**
- A Design Activity
  - Dynamic Voltage Scaling
- Summary

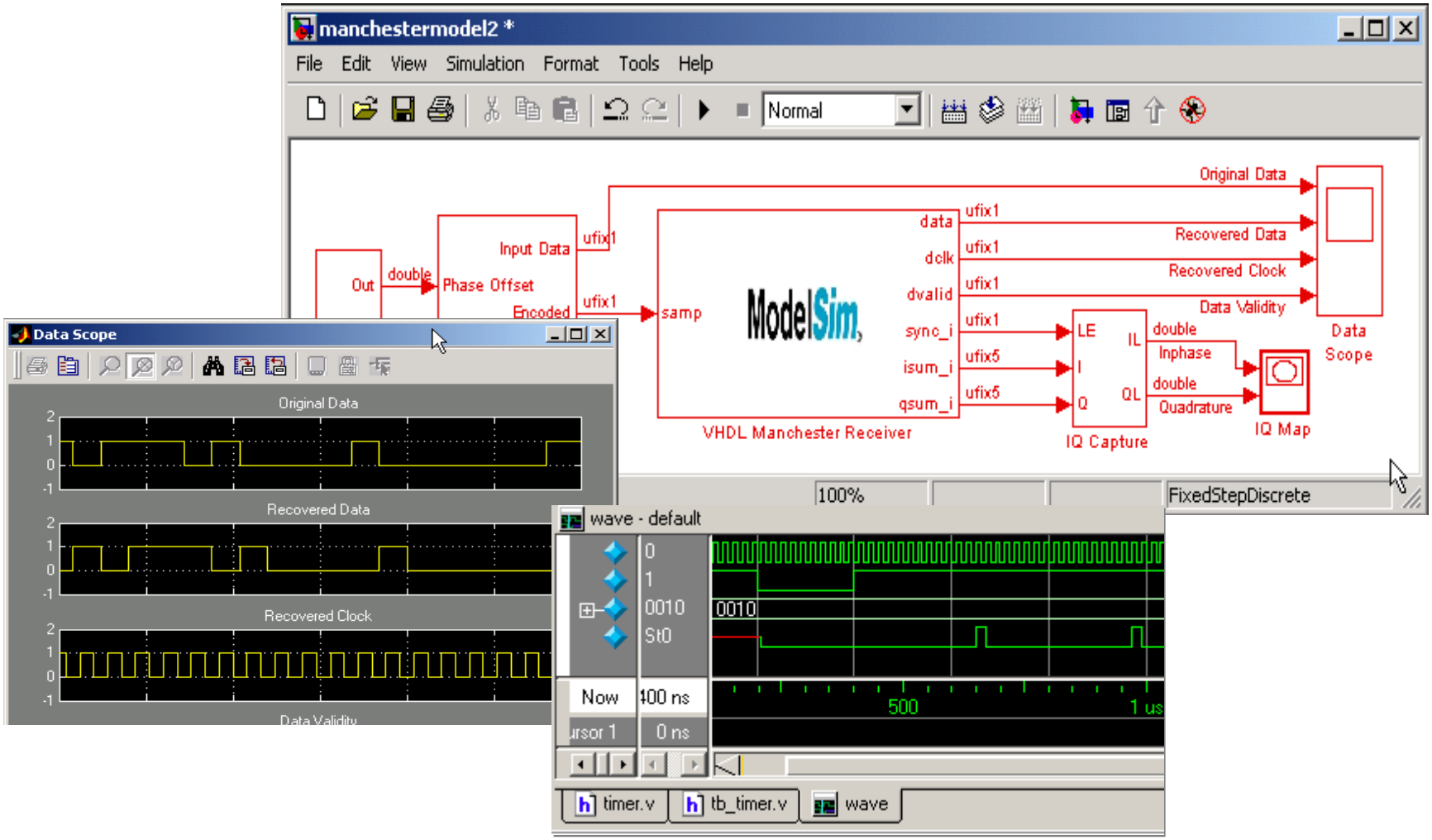
# Demo

Live MATLAB Demo



- Edge detection demo
  - Design space exploration using floating point
  - Conversion to fixed point
  - Elaboration to facilitate streaming data
  - Co-simulate with HDL

# Simulink co-simulation



# Link for ModelSim allows engineers to share models instead of I/O vectors.

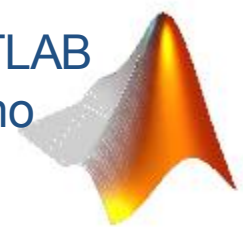
- The HDL is verified in the context of an entire system and not just as a stand-alone component
- System performance metrics, e.g. Packet Error rate (PER), Bit Error Rate (BER), Signal to Noise (S/N) ratio can be measured

# Agenda

- Introduction
- Embedded Systems Design
- Demo
- **A Design Activity**
  - **Dynamic Voltage Scaling**
- Summary

# Dynamic Voltage Scaling

Live MATLAB Demo



- Simulate AT90S8535 microcontroller
- Dynamic Voltage Scaling (DVS) based on online gradient estimation
  - Infinitesimal perturbation analysis (IPA)
- Average cost per job
  - $J(\theta) = w\ P(\theta) + S(\theta)$
  - $J(\theta) = w\ c_2[V_t / (1 - c_1/\theta)]^2 + S(\theta)$
  - $\theta$, average service time; w, weighting; P, average energy consumption; S, average system time for a job; $c_1$ and $c_2$, device constants; $V_t$, minimum input voltage

# Agenda

- Introduction
- Embedded Systems Design
- Demo
- A Design Activity
  - Dynamic Voltage Scaling
- **Summary**

# Summary

- Integrate system level design with implementation
  - Cycle accurate simulation
- No duplication of testbench design effort
- Analysis of system level properties