Architectures Session

Godson-T: A Teraflops Many Core Design for Next-Generation High Performance Computing

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Abstract

Godson-T is a processor prototype of many-core architecture designed with 65nm CMOS technology. It targets highly parallelizable applications which require high computational throughput.

Godson-T has 64 homogeneous, in-order and dual-issue processing cores. The target frequency of each core is 1GHz. The RISC-like processing core supports 32-bit MIPS ISA (user-level) with synchronization instruction extensions. One floating-point arithmetic operation and one floating-point multiply-add operation can be issued to corresponding fully-pipelined function units in a cycle, so the peak single-precision floating-point performance of Godson-T is 192GFLOPS. Each processing core has a 16KB 2-way set-associative private instruction cache and a 32KB local memory. The local memory functions as a 32KB 4-way set-associative private data cache in default. It can also be configured as an explicitly-controlled Scratchpad Memory (SPM), or a hybrid of cache and SPM. A Data Transfer Agent (DTA) is built in each core for fast data communication. In addition, there are 16 address-interleaved L2 cache banks (256KB each) distributed along four sides of the chip. The L2 cache is shared by all processing cores and can serve up to 64 cache accessing requests in total. Four L2 cache banks in the same side of the chip share a memory controller.