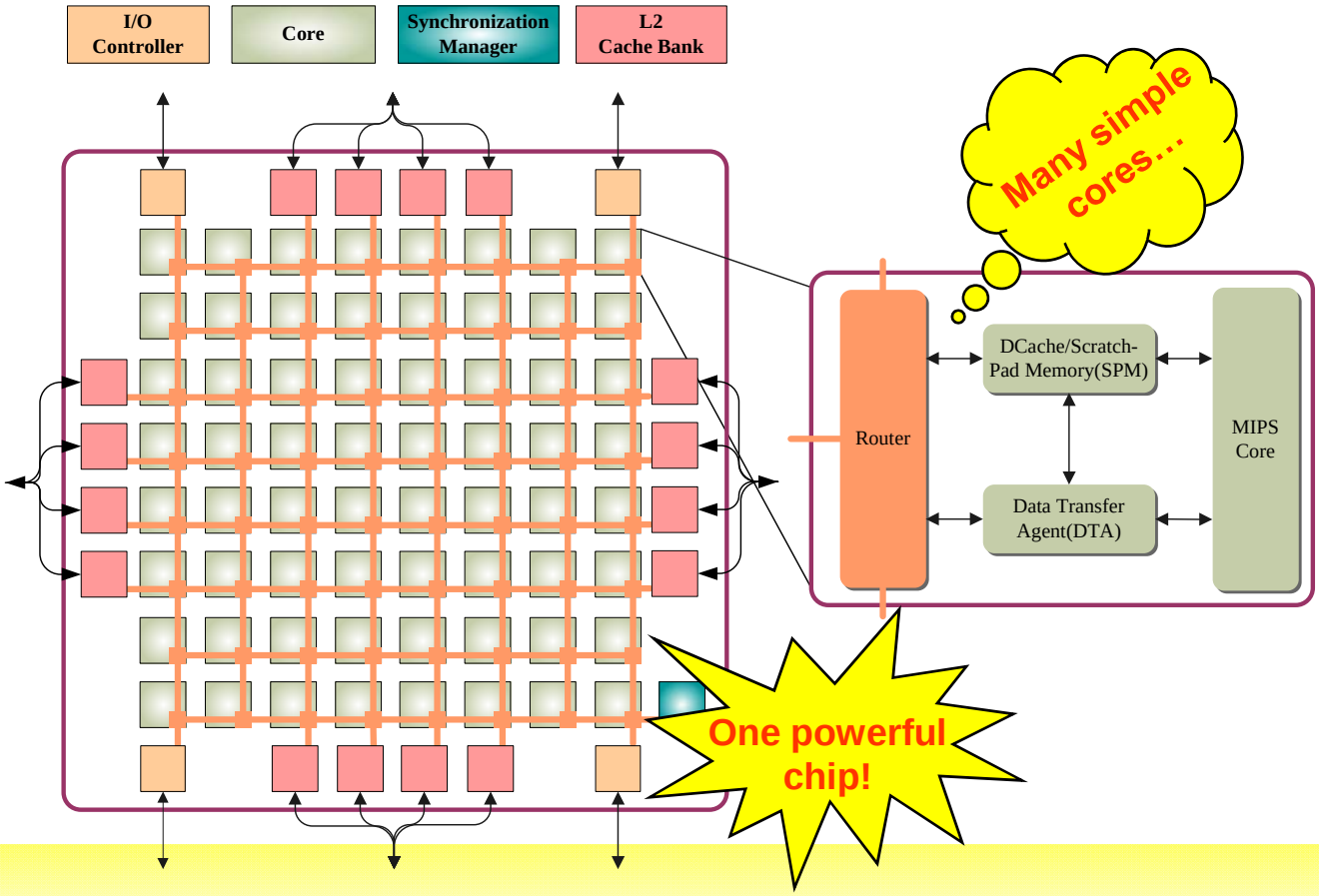
Godson-T: A Teraflops Many Core Design for the Next-Generation High Performance Computing



Godson-T is a processor prototype of many-core architecture designed with 65nm CMOS technology. It targets highly parallelizable applications which require high computational throughput. The figure above gives the overview of the Godson-T processor architecture.

Godson-T has 64 homogeneous, in-order and dual-issue processing cores connected by a 8x8 mesh network. The target frequency of each core is 1GHz. The RISC processing core supports 32-bit MIPS ISA (user-level) with synchronization instruction extensions. One floating-point arithmetic operation and one floating-point multiply-add operation can be issued to corresponding fully-pipelined function units in a cycle, so the peak single-precision floating-point performance of Godson-T is 192GFLOPS. For now, the design is running on FPGA.

Features:

- One chip with ***64 dual-issue cores*** connected by an ***8x8 mesh*** network
- ***Configurable on-chip memory*** that can be SPM or/and data cache
- ***Fast task creation & termination*** within tens of cycles
- Fast locks and barriers enabled by a ***synchronization manager*** node
- Fast memory access enabled by ***software managed SPM***
- ***Fine grain synchronization*** enabled by Full/Empty bits with SPM
- Memory wall break via asynchronous memory access enabled by on-chip ***DMA***s
- Efficient inter-core communication enabled by ***row/column broadcasting***

Advanced Micro-System team
先进微系统组
Institute of Computing Technology, Chinese Academy of Sciences
中科院计算所
http://ams.ict.ac.cn
zhanghao@ict.ac.cn