

Architectures Session

## MORPHEUS – Heterogeneous Reconfigurable SOC

Alberto Rosti<sup>1</sup>, Philippe Bonnot<sup>2</sup>, Stelios Perissakis<sup>3</sup>, Kostantinos Potamianos<sup>3</sup>, Wolfram Putzke-Röming<sup>4</sup>, Nikolaos S. Voros<sup>5</sup>

<sup>1</sup>STMicroelectronics, Agrate Brianza, Italy, [alberto.rosti@st.com](mailto:alberto.rosti@st.com)

<sup>2</sup>Thales Research & Technology, Palaiseau, France, [philippe.bonnot@thaligroup.com](mailto:philippe.bonnot@thaligroup.com)

<sup>3</sup>INTRACOM S.A. Telecom Solutions, 19.5 Km Markopoulo Avenue, PO Box 68, 19002, Attika, Peania, Greece, [{sper,cpot}@intracom.gr](mailto:{sper,cpot}@intracom.gr)

<sup>4</sup>Deutsche Thomson OHG – Corporate Research, Hannover, Germany, [wolfram.putzke-roeming@thomson.net](mailto:wolfram.putzke-roeming@thomson.net)

<sup>5</sup>Technological Educational Institute of Mesolonghi, National Road Nafpaktos-Antirio (Varia), 30300 Nafpaktos, Consultant to INTRACOM S.A. Telecom Solutions, [voros@teimes.gr](mailto:voros@teimes.gr)

### Abstract

MORPHEUS is a European project started in 2006; it proposes a technology breakthrough in the embedded computing field. MORPHEUS copes with two main challenges. The first deals with raising the design complexity of state of the art applications. The second challenge is related to design productivity that inhibits appropriate exploitation of silicon technology. MORPHEUS is developing a global solution based on a heterogeneous System-on-Chip (SoC) platform which provides the disruptive technology of dynamically reconfigurable computing including a software oriented design flow and a consistent toolset. MORPHEUS strives to establish the European foundation for a new concept of flexible “domain focused platforms”, which are positioned between general purpose flexible hardware, SoC and general purpose processors. MORPHEUS provides breakthroughs in performance and cost-effectiveness for embedded computing systems. The main innovative point of MORPHEUS is that in 2009 it will provide a silicon chip demonstrator in 90nm technology. The chip will be tested on a set of target applications.

