

# Dynamic structure modelling for Causal Block Diagrams

Master Thesis by Yves Maris

Promotors: Fernando Barros, Hans Vangheluwe

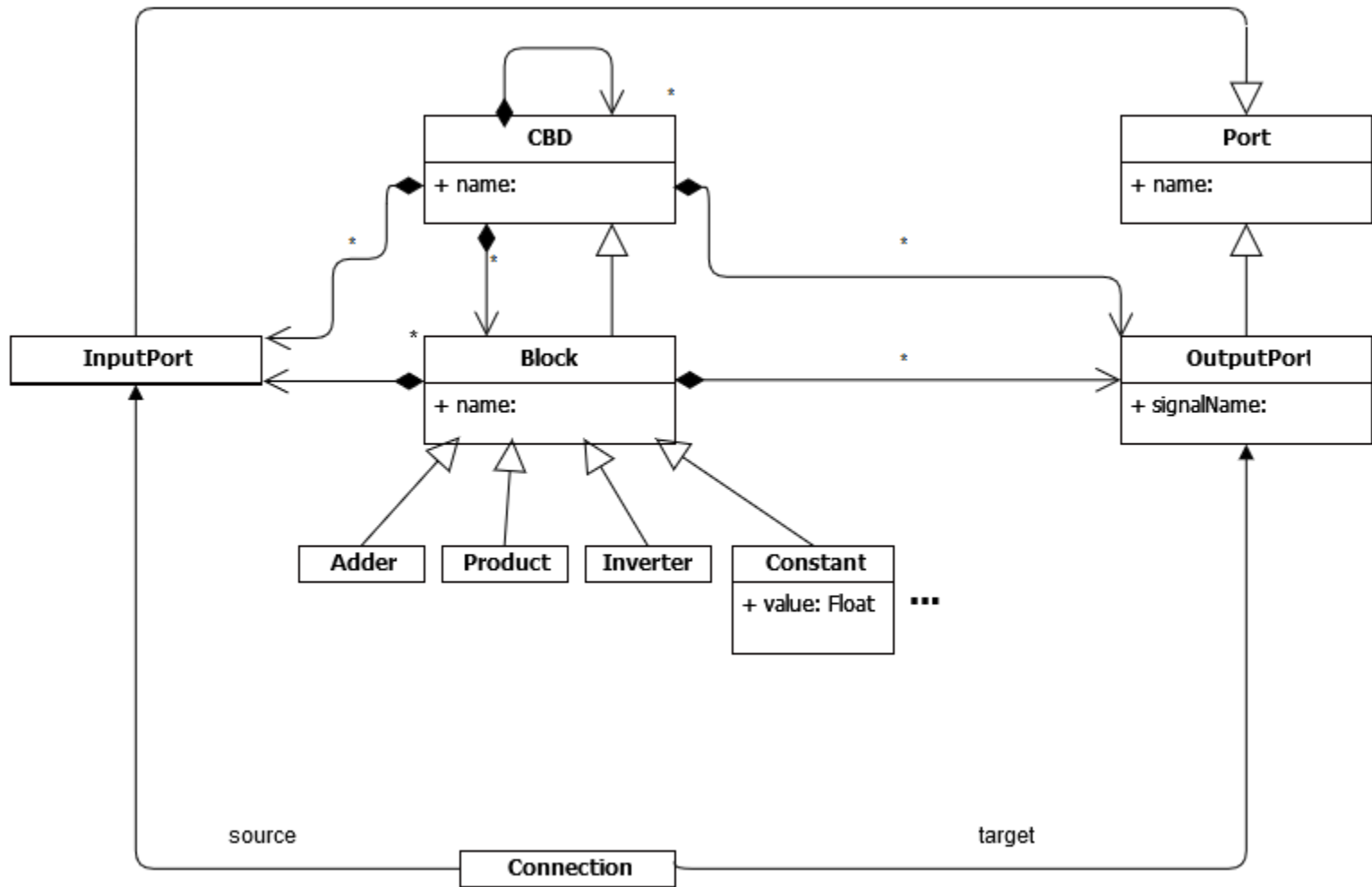
# Overview

- Background: Causal Block Diagrams
  - Syntax
  - Semantics
- Problem statement
- Dynamic structure CBD
  - Syntax
  - Semantics
- Implementation
- Case study: elevator model

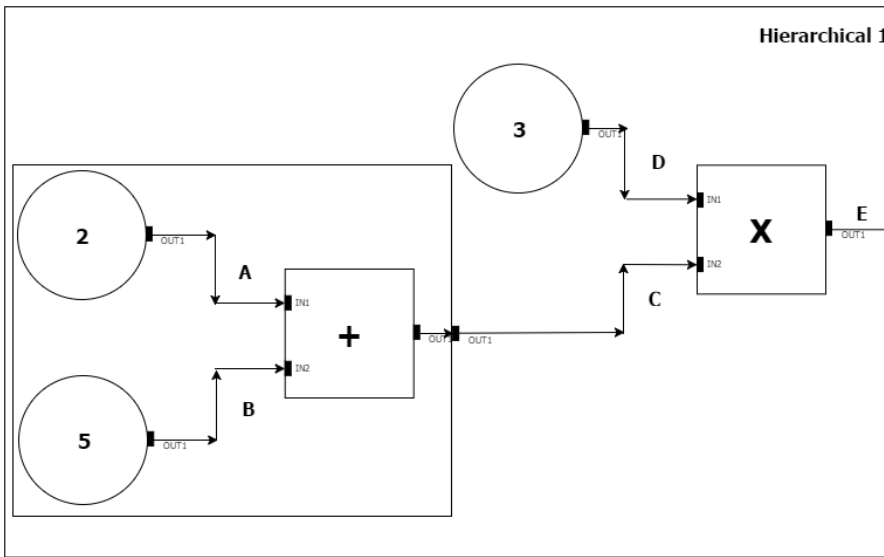
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# Causal Block Diagrams Abstract Syntax



# Causal Block Diagrams Visual Syntax



Name	Block	Name	Block
Adder block		AND block	
Product block		OR block	
Modulo block		Greater than block	
NegatorBlock		Equals block	
InverterBlock		NOT Block	
SquarerootBlock			
Ln block			

Name	Block
Integrator block	
Derivator block	

Name	Block
Delay block	

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# Causal Block Diagrams semantics

**Algorithm 2:** Operational semantics CBD ( adaptation from [8] and [15])

```
Data: cbd  
Result: Behaviour trace  
1 logicalTime = 0;  
2 flatcbd = FLATTEN(cbd);  
3 while not end_condition do  
4   | schedule = LOOPDETECT(DEPGRAPH(flatcbd));  
5   | for block in schedule do  
6   |   | COMPUTE(block)  
7   | logicalTime = logicalTime +  $\delta t$ 
```

# Background: flattening

- Purely syntactical
- Needed for loop detection



# Background: Evaluation Order

- Dependencies between blocks
- Topological sort

# Loop detection

- Strong component algorithm
- Use gaussian solver for implicit solution

**Algorithm 1:** Loop detection

```
Data: graph  
Result: The strong components within graph  
1 topSort(graph);  
2 revGraph = reverseEdges(graph);  
3 strongComponents=[];  
4 for node in revGraph do  
5   | Mark node as visited;  
6 while !isEmpty(revGraph) do  
7   | startNode = highestOrderNumber(revgraph);  
8   | component = dfsCollect(startNode,revNode);  
9   | appendResult(component);  
10  | revGraph.remove(component);
```

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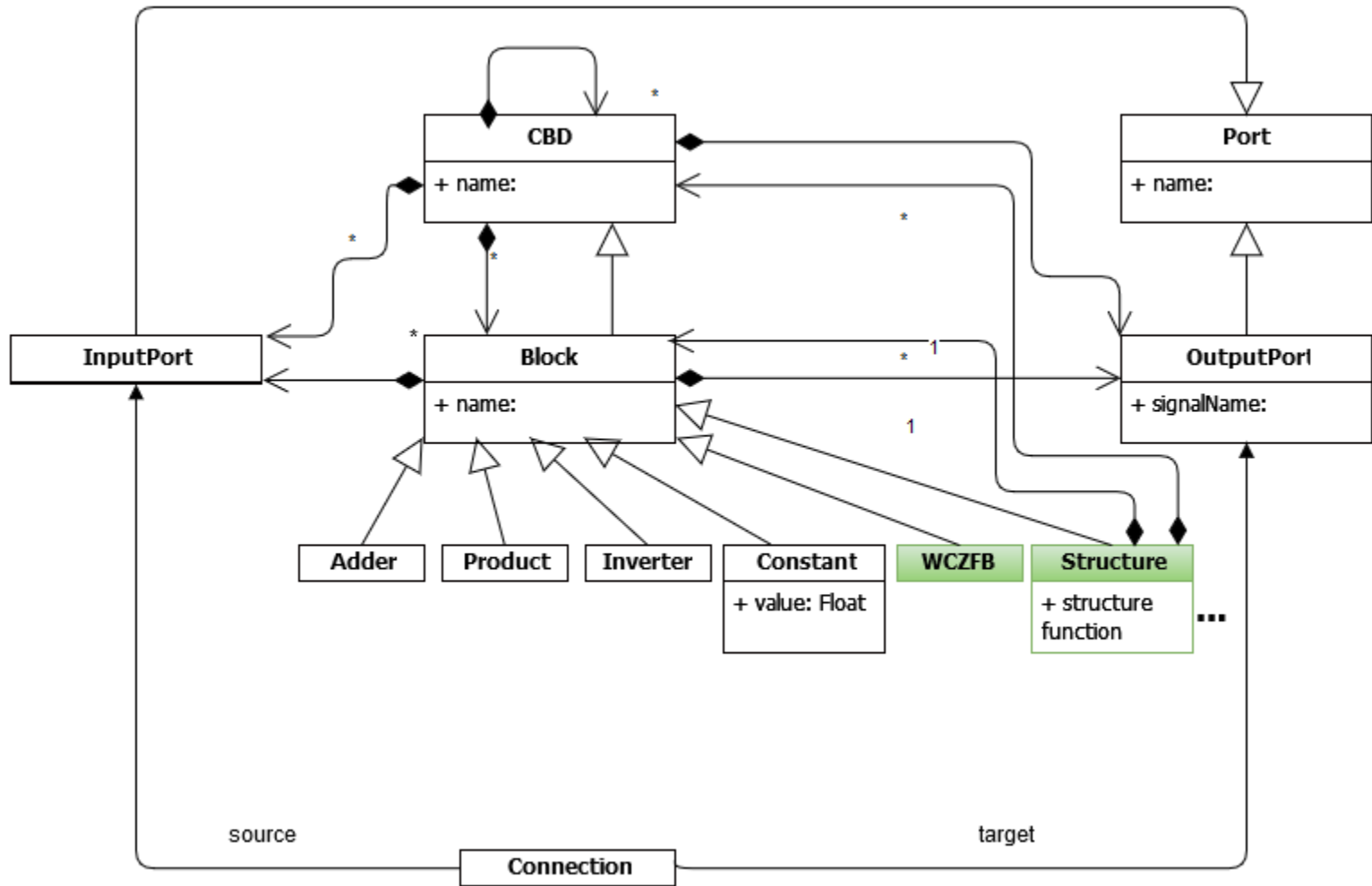
# Problem Statement

- Expressiveness limited by fixed structure
- Changing model during simulation
- Staying consistent with CBD constructs

# Schedule

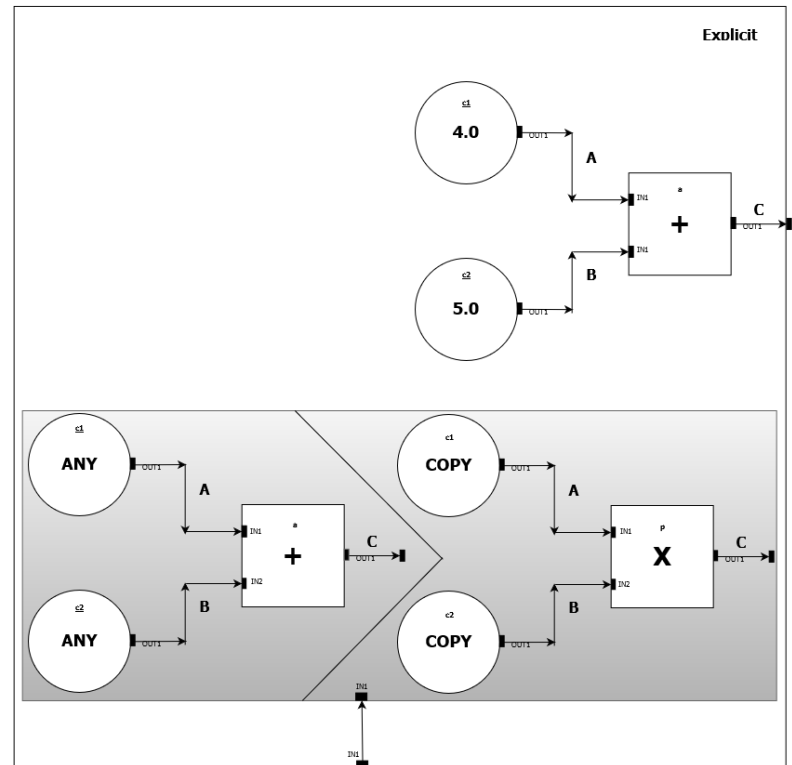
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- **Dynamic structure CBD**
  - **Syntax**
  - Semantics
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# Abstract Syntax



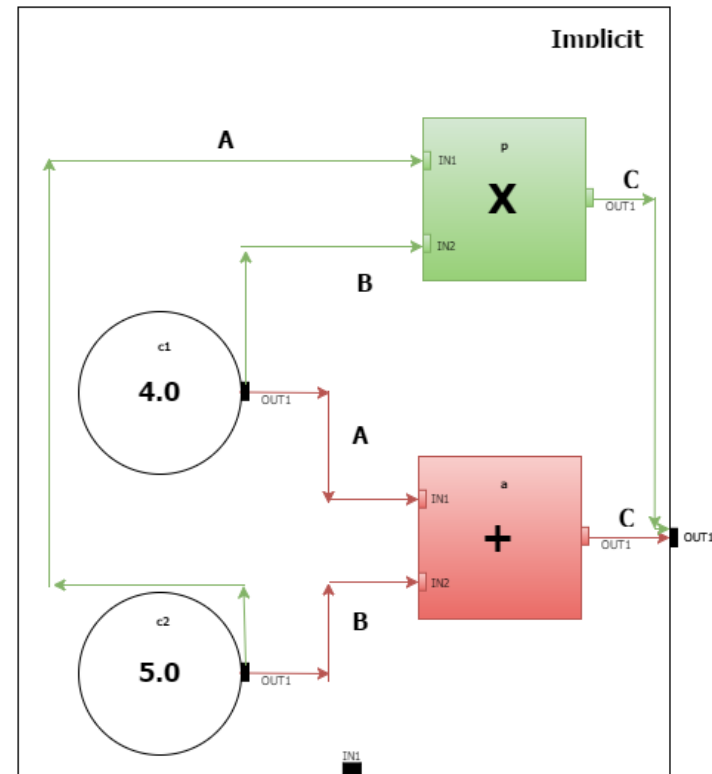
# Visual syntax: explicit representation

- Reuse of existing graph transformation syntax
- Left-hand side before
- Right-hand side after
- Trigger through input port



# Visual syntax: implicit representation

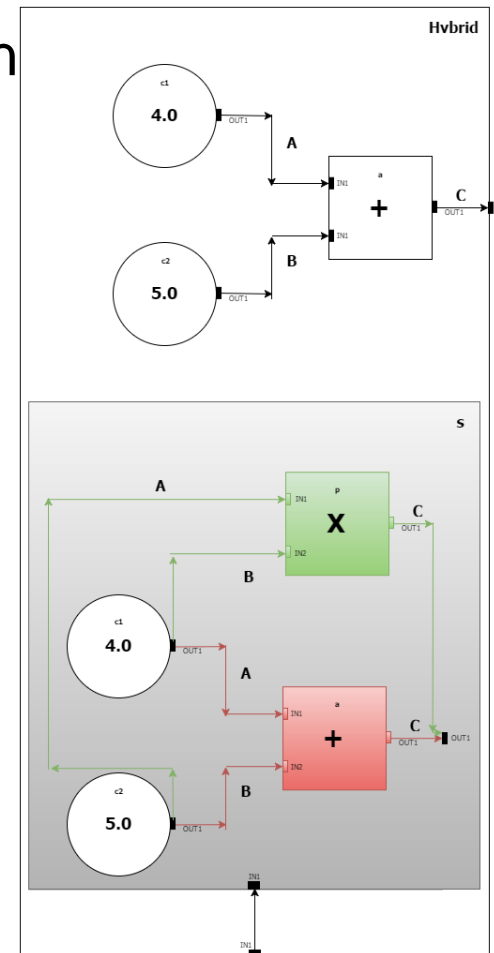
- Trigger received through CBD input port
- Added structures: green
- Removed structures: red





# Visual syntax: hybrid representation

- Mix between implicit and explicit representation
- Implicit representation separated by block
- Simulated model isolated



# Visual syntax: comparison

- Implicit representation not expressive enough
- Hybrid representation
  - Same expressiveness as explicit representation
  - More compact

	Implicit	Explicit	Hybrid
Removing connections	X	X	X
Adding connections	X	X	X
Removing Blocks	X	X	X
Adding Blocks	X	X	X
Reinitialising new structures	-	X	X
Higher order structural change	-	X	X
Pattern matching	-	X	X

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  - Visual syntax
  - **Semantics**
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# Related work

## – Hybrid CBD

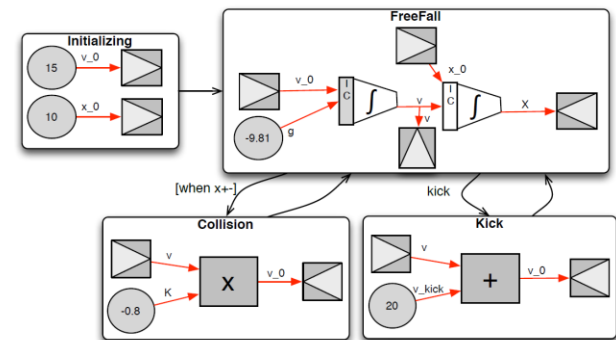
- Mustafiz, Sadaf, et al. "Towards Modular Language Design Using Language Fragments: The Hybrid Systems Case Study." *Information Technology: New Generations*. Springer International Publishing, 2016. 785-797.
  - Uses signal crossing

## – Dynamic structure DEVS (DSDEVS)

- Barros, Fernando J. "Modeling formalisms for dynamic structure systems." *ACM Transactions on Modeling and Computer Simulation (TOMACS)* 7.4 (1997): 501-515.

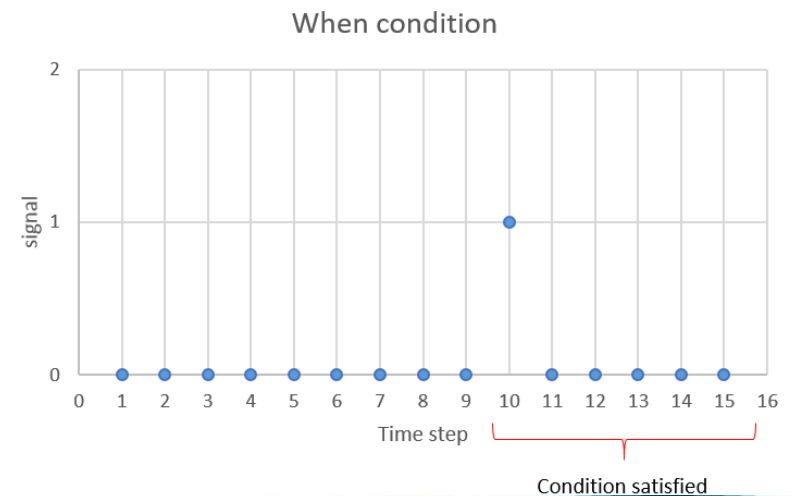
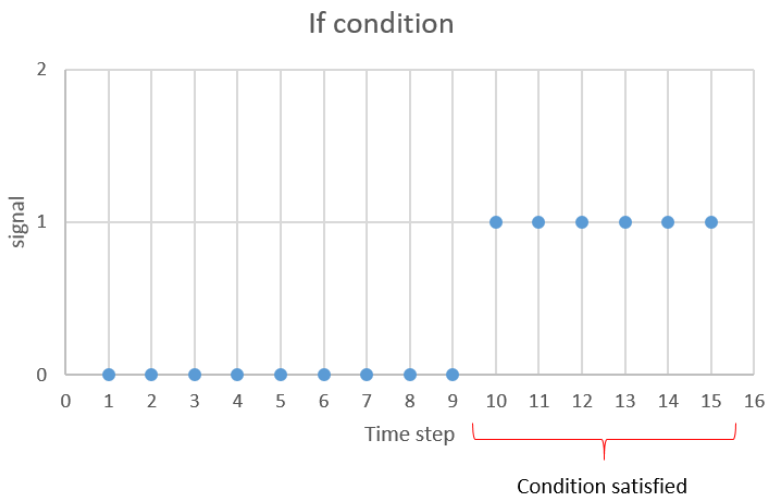
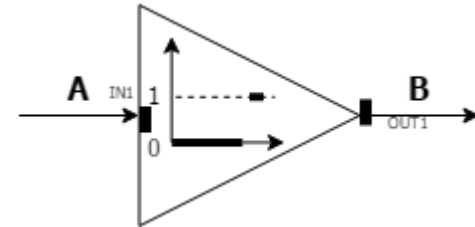
## – Heterogeneous flow systems

- Barros, Fernando J. "Dynamic structure multiparadigm modeling and simulation." *Simulation (TOMACS)* 13.3 (2003): 259-275.
  - Use of model executive



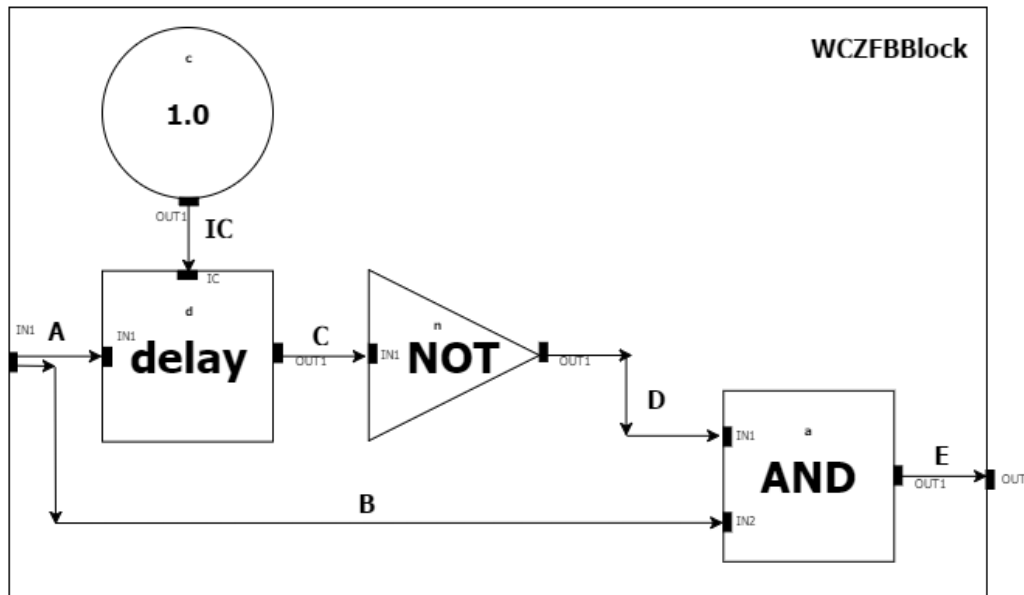
# Triggering a change: zero crossing

- Piecewise constant signal to “event”
- Pre and post condition
- Implemented using basic blocks



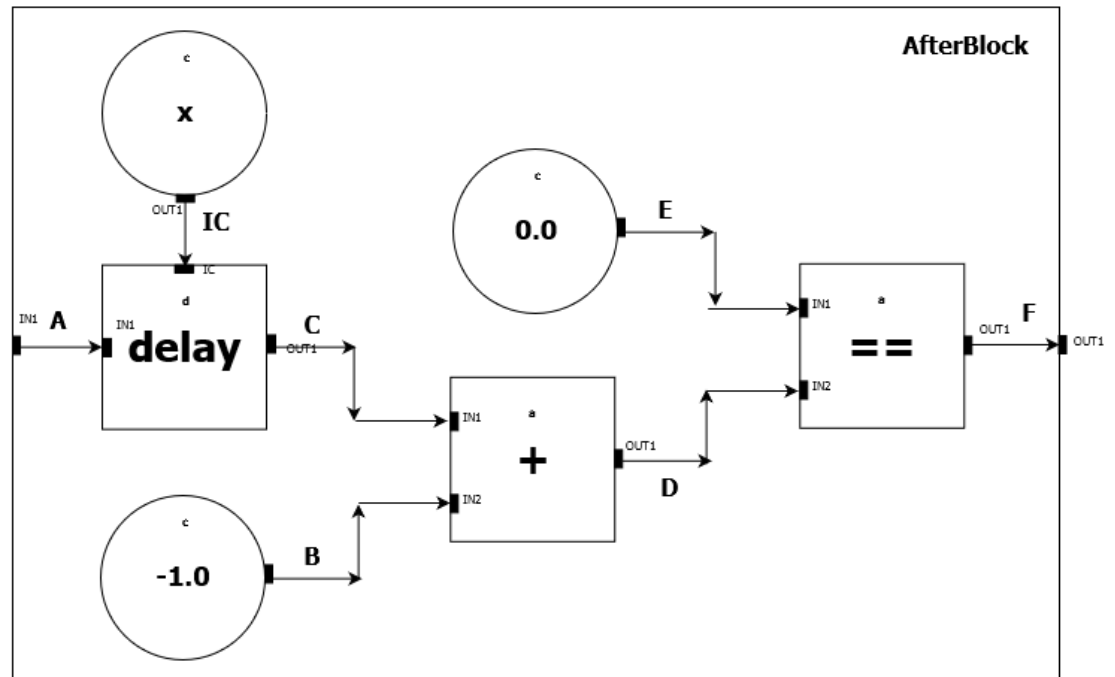
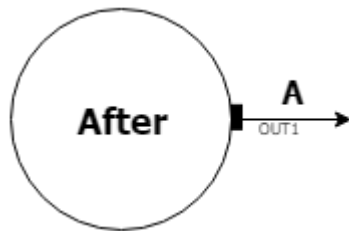
# Triggering a change: zero crossing

- Signal must cross zero from below
  - Previous iteration: condition must be not satisfied
  - Current iteration: condition must be satisfied



# Triggering a change: timed event

- Generating “event” after a fixed number of timesteps
- Value determined when initialised



# Modeling a change: structure block

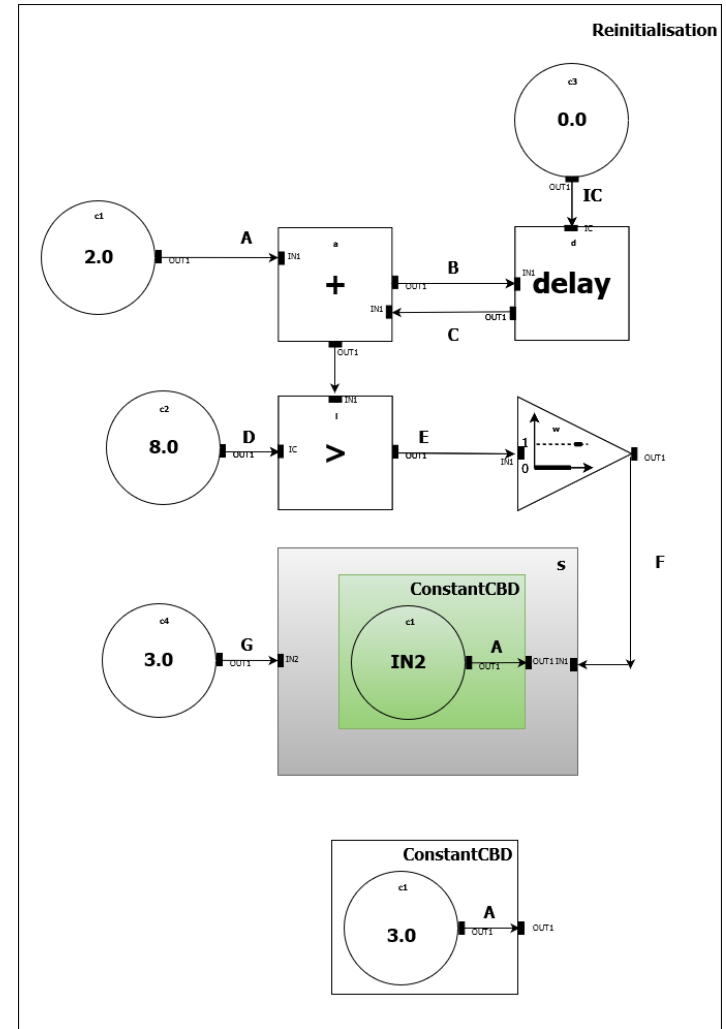
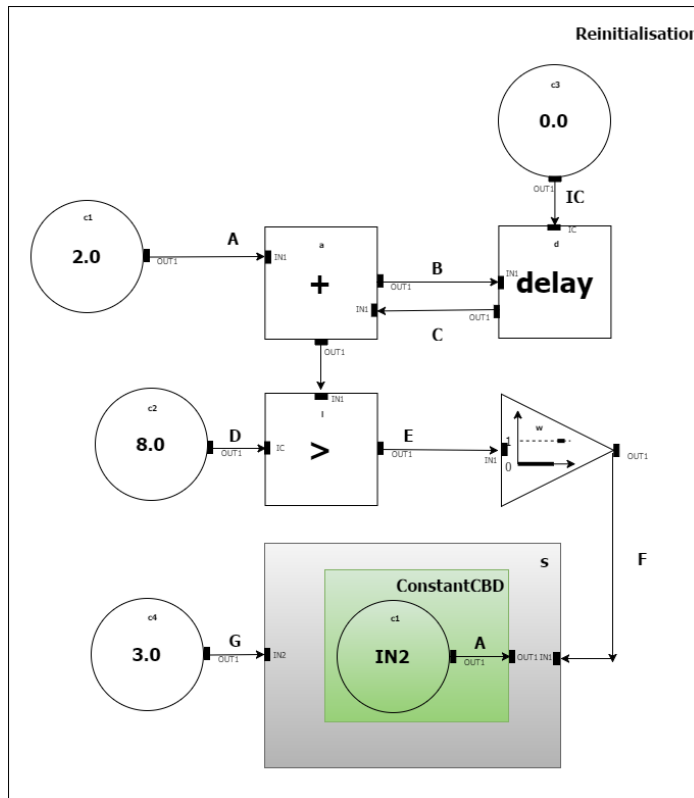
- Features of a dynamic structure formalism
  - Identification of existing structures
  - Creation of new structures
  - Removal of existing structures
  - Initialisation of values



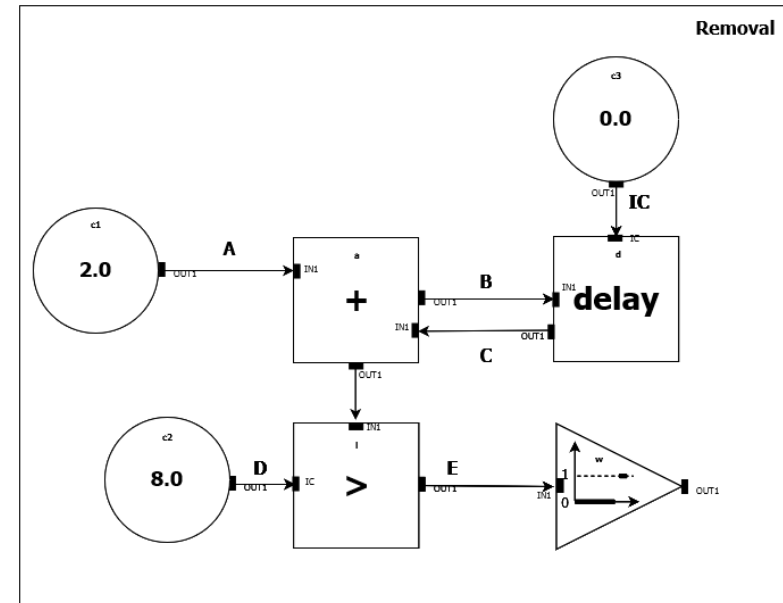
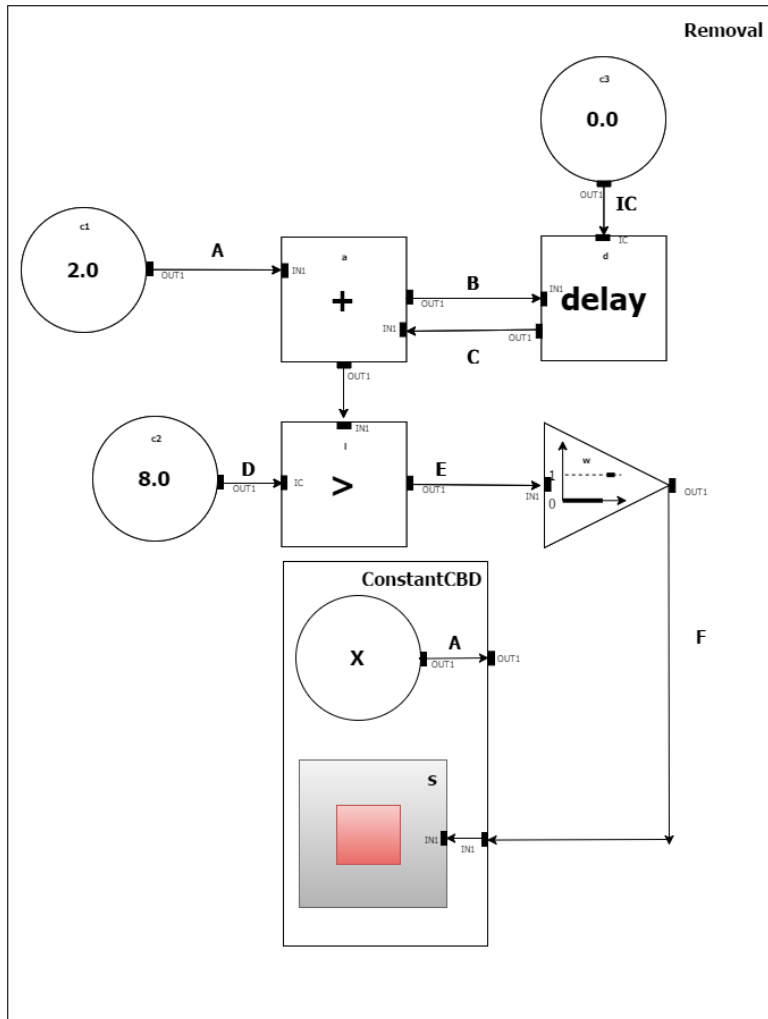
# Modeling a change: structure block

- Structure block = adapted CBD specification
- Structure function for modelling change
- Multiple input/ no output ports
  - Default 1: event that triggers a change
  - Other input ports for initialisation of values
- Changes apply only to one CBD! (hierarchical)

# Modeling a change: examples



# Modeling a change: examples



# Adapted operational semantics

## Algorithm 3: Operational semantics dynamic structure CBD

```

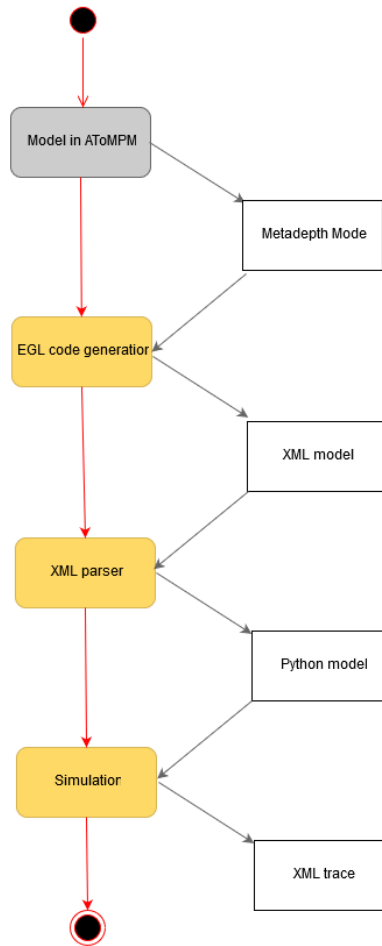
Data: cbd
Result: Behaviour trace
1 logicalTime = 0;
2 while not end_condition do
3   | flatcbd = FLATTEN(cbd);
4   | schedule = LOOPDETECT(DEPGRAPH(flatcbd)) structureBlocks =
   | COLLECTSTRUCTBLOCKS(schedule);
5   | for block in schedule do
6     | flatcbd = COMPUTE(block, flatcbd)
7   | for block in structureBlocks do
8     | cbd = COMPUTE(block, cbd)
9   | logicalTime = logicalTime +  $\delta t$ 

```

# Overview

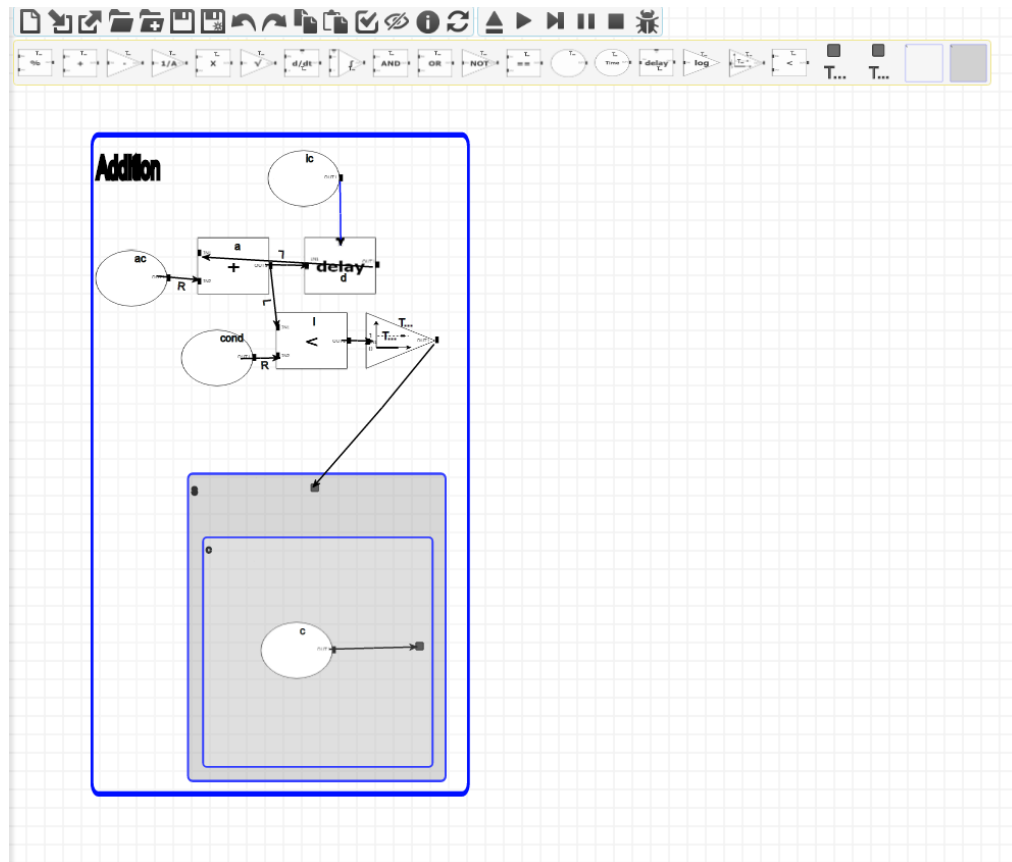
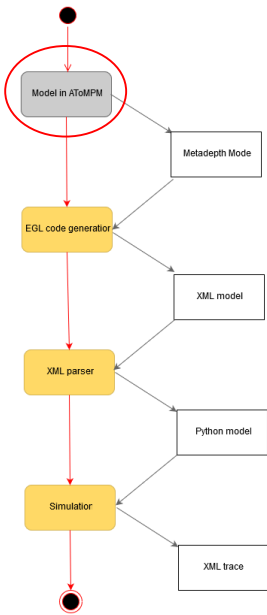
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# Implementation



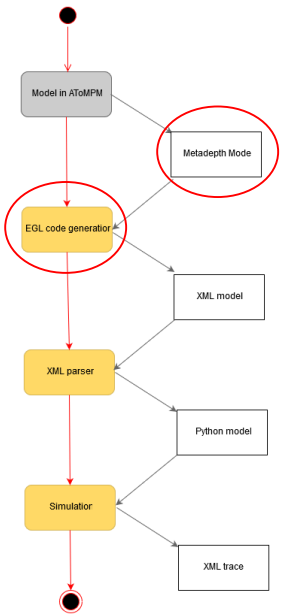
# Implementation: AToMPM

- Visual modeling environment



# Metadepth

- Exported AToMPM model using built in functionality
- Supports EGL for code generation



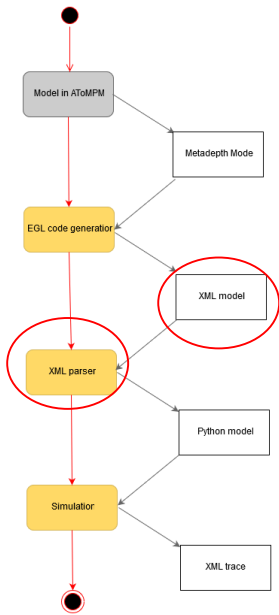
```

72 type = "default";
73 }
74 contents contents_14 {
75 src = CBD_10;
76 dst = ConstantBlock_13;
77 }
78 IC IC_15 {
79 src = ConstantBlock_13;
80 dst = DelayBlock_11;
81 type = "default";
82 }
83 AdderBlock AdderBlock_19 {
84 name = "a";
85 position = [0,0];
86 type = "default";
87 }
88 contents contents_20 {
89 src = CBD_10;
90 dst = AdderBlock_19;
91 }
92 Delay_IN Delay_IN_21 {
93 src = AdderBlock_19;
94 dst = DelayBlock_11;
95 type = "default";
96 }
97 LeftOperand LeftOperand_22 {
98 src = DelayBlock_11;
99 dst = AdderBlock_19;
100 type = "default";
101 }
102 ConstantBlock ConstantBlock_23 {
103 value = 2;
104 name = "ac";
105 position = [0,0];
106 type = "default";
107 }
108 contents contents_25 {
109 src = CBD_10;
  
```



# XML

- Readable models
- Consistent declarations
- Remove tags

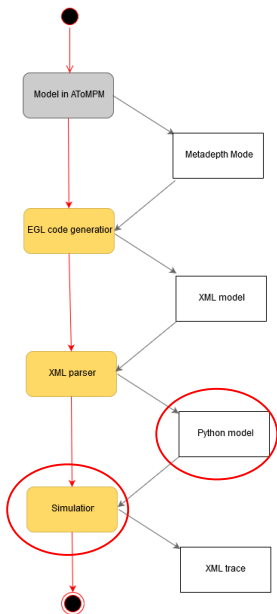


```

301 <Connection from_block = "int" to_block = "OUT1"/>
302 </CBD>
303 <CBD name = "BallyY" num_input_ports = "2" num_output_ports = "1">
304 <Block type = "ConstantBlock" block_name = "dt" value = "0.005"/>
305 <Block type = "ConstantBlock" block_name = "radius" value = "10"/>
306 <Block type = "ConstantBlock" block_name = "y0" min_value = "125.0" max_value = ">
307 <Block type = "IntegratorBlock" block_name="int"/>
308 <Block type = "LessThanBlock" block_name = "l1"/>
309 <Block type = "WCZFBlock" block_name = "w1"/>
310 <Block type = "LessThanBlock" block_name = "l2"/>
311 <Block type = "WCZFBlock" block_name = "w2"/>
312 <Block type = "AdderBlock" block_name = "a"/>
313 <Block type = "AdderBlock" block_name = "a1"/>
314 <Block type = "NegatorBlock" block_name="n"/>
315 <CBD name = "BallSpeedY" num_input_ports = "2" num_output_ports = "1">
316 <Block type = "ConstantBlock" block_name = "c0" value = "0"/>
317 <Block type = "ConstantBlock" block_name = "dt" value = "0.05"/>
318 <Block type = "ConstantBlock" block_name = "ic" value = "1"/>
319 <Block type = "ConstantBlock" block_name = "a" value = "50"/>
320 <Block type = "ConstantBlock" block_name="vy" min_value = "50.0" max_value = ">
321 <Block type = "IntegratorBlock" block_name="i"/>
322 <Block type = "NegatorBlock" block_name="neg"/>
323 <Block type = "AndBlock" block_name="and1"/>
324 <Block type = "AndBlock" block_name="and2"/>
325 <Block type = "OrBlock" block_name="or"/>
326 <Block type = "GreaterThanBlock" block_name = "g"/>
327 <Block type = "LessThanBlock" block_name = "l"/>
328 <Block type = "StructureBlock" block_name="resetIntegrator" num_inputs = "2">
329 <Remove block_name="i"/>
330 <Remove block_name="vy"/>
331 <Block type = "IntegratorBlock" block_name="i" />
332 <Block type = "ConstantBlock" block_name="vy" value="IN2" />
333 <Connection from_block = "dt" to_block = "i" input_port_name = "delta_t"/>
334 <Connection from_block = "vy" to_block = "i" input_port_name = "IC" />
335 <Connection from_block = "a" to_block = "i"/>
336 <Connection from_block = "i" to_block = "OUT1"/>
337 <Connection from_block = "i" to_block = "neg"/>
  
```

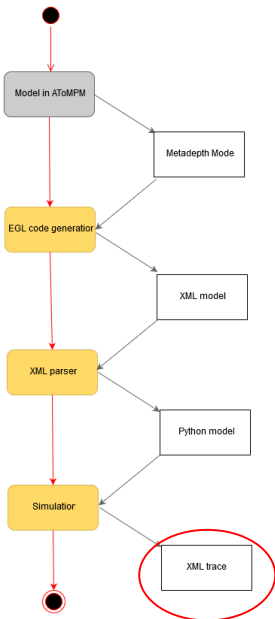
# Python

- Parser generates code including structure functions
- Simulator implemented in python
  - Extended CBD simulator from MOSIS course



# Debugging

- Test driven development
- Traces



```

<TimeStep iteration = 4>
  <Output type = "InverterBlock" block_name = "ic" value = 0.0/>
  <Output type = "DelayBlock" block_name = "d" value = 8.0/>
  <Output type = "InverterBlock" block_name = "ac" value = 2.0/>
  <Output type = "AdderBlock" block_name = "a" value = 10.0/>
  <Output type = "InverterBlock" block_name = "cond" value = 8.0/>
  <Output type = "GreaterThanBlock" block_name = "g" value = 1/>
  <Output type = "WireBlock" block_name = "w.IN1" value = 1/>
  <Output type = "DelayBlock" block_name = "w.d1" value = -1/>
  <Output type = "NotBlock" block_name = "w.n" value = 1/>
  <Output type = "AndBlock" block_name = "w.a" value = 1/>
  <Output type = "WireBlock" block_name = "w.OUT1" value = 1/>
  <Output type = "WireBlock" block_name = "OUT1" value = 10.0/>
  <Output type = "InverterBlock" block_name = "w.delayic" value = -1/>
  <Block type = "OutputPortBlock" block_name = "OUT1" time_offset = 5/>
  <CBD name = "ConstantCBD0" time_offset = 5/>
  <Block type = "ConstantBlock" block_name = "c" value = 2.0 time_offset = 5/>
</TimeStep />
  
```

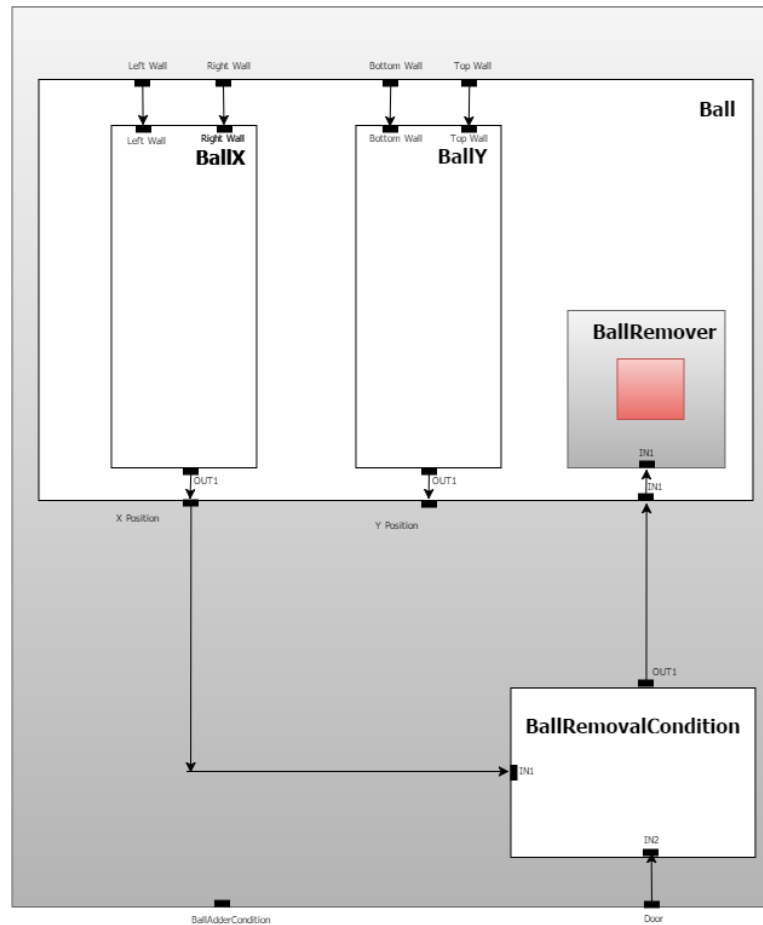
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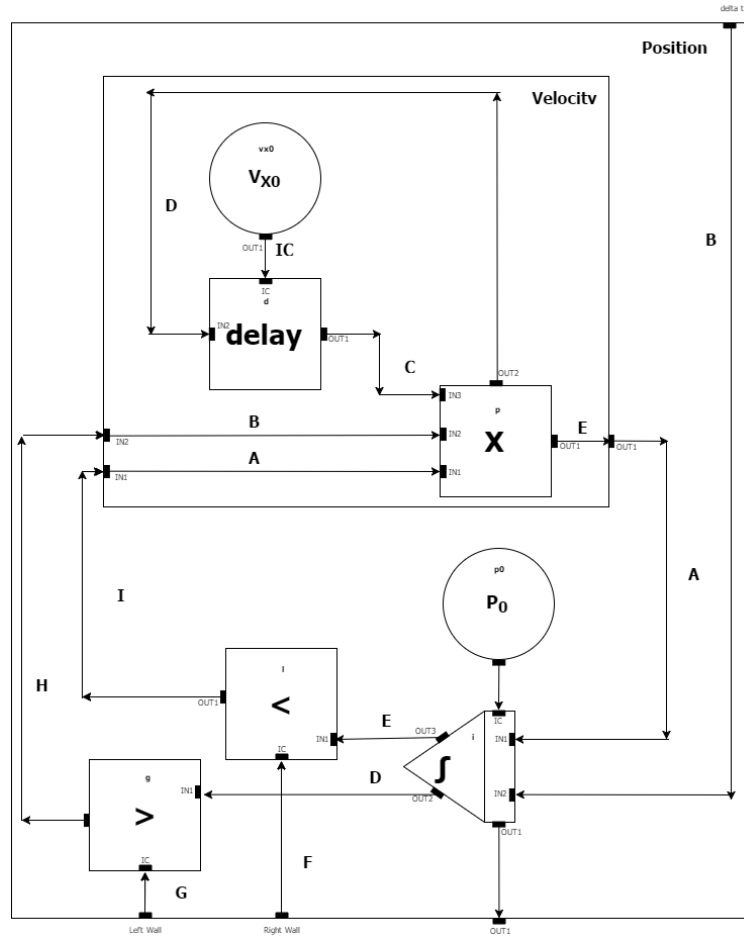
# Case Study

- Balls in elevator
- Doors open when elevator reaches floor
- Balls can enter and leave elevator through door

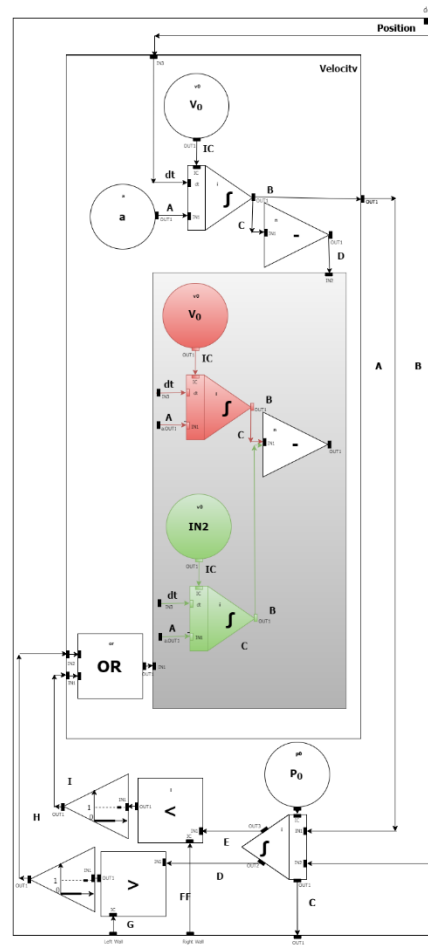
# Modeling a Ball



# Position with constant velocity

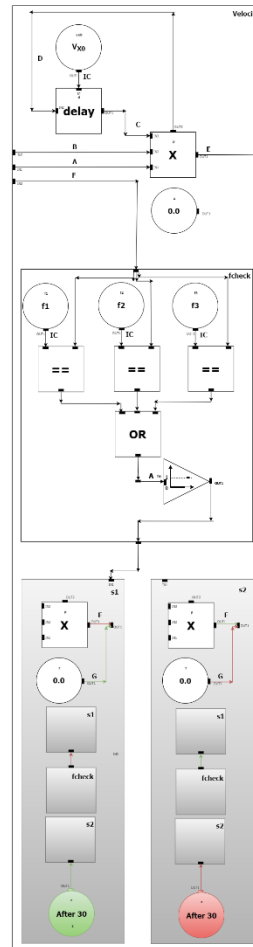


# Position with constant acceleration

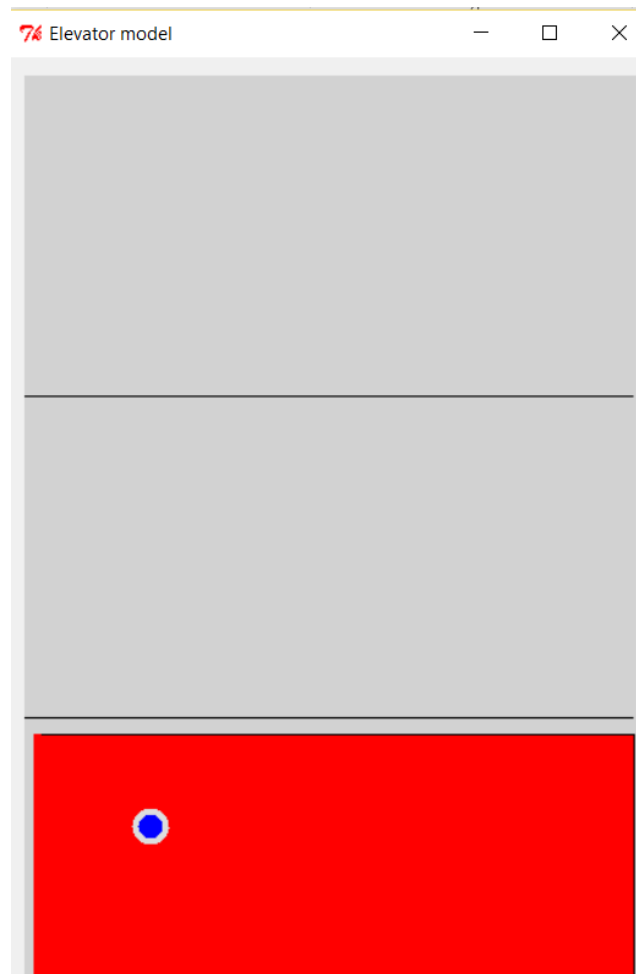




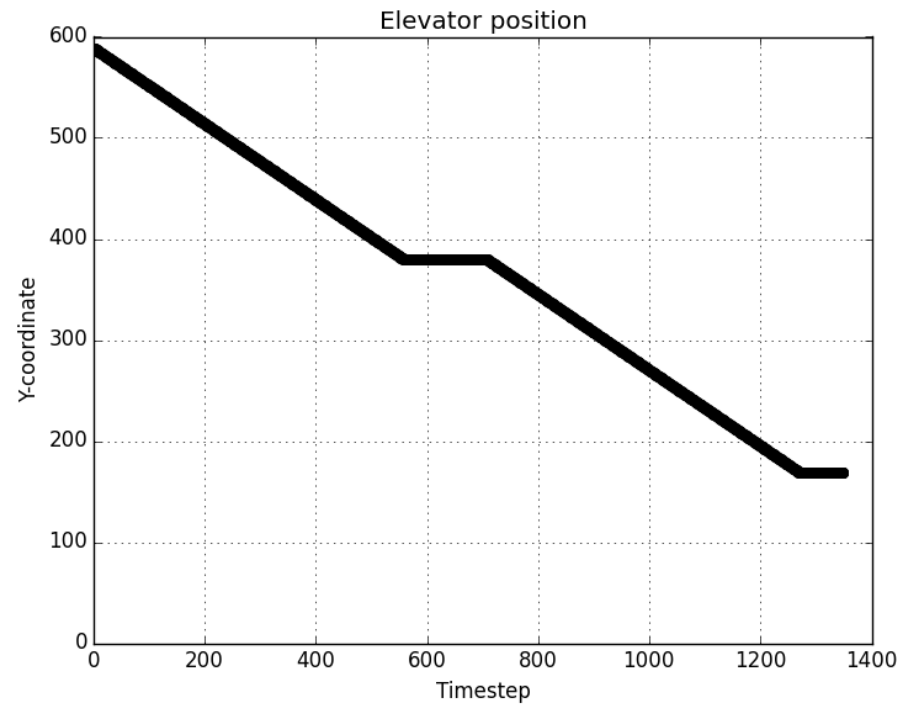
# Velocity CBD for elevator wall



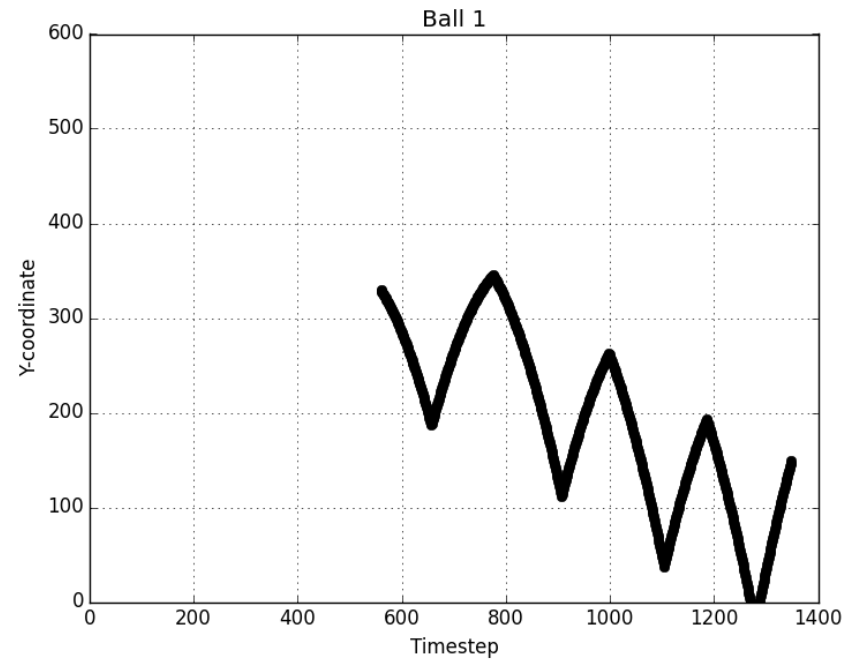
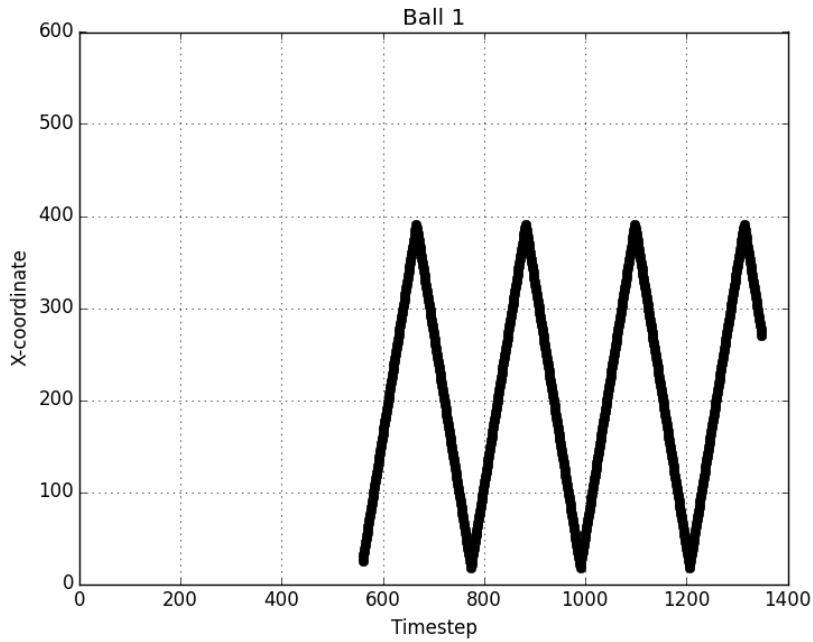
# Demo



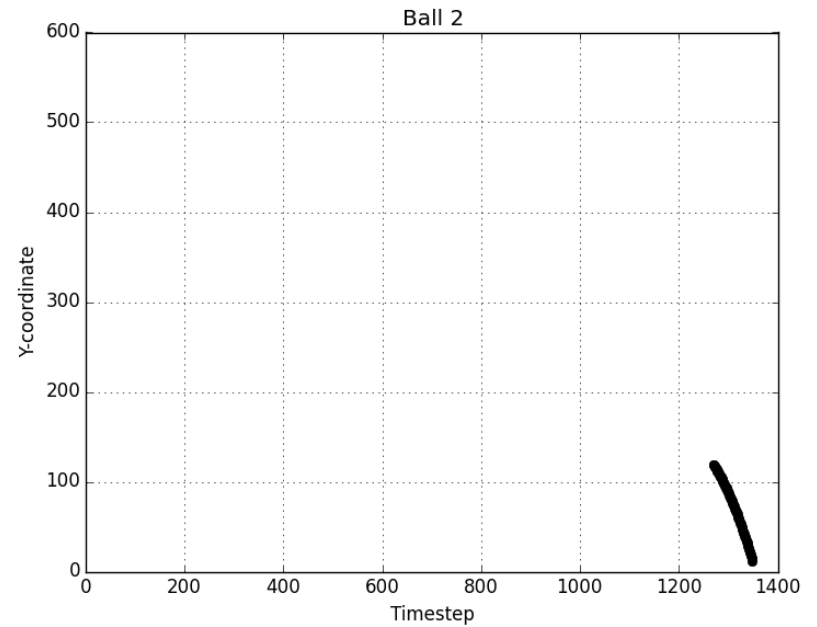
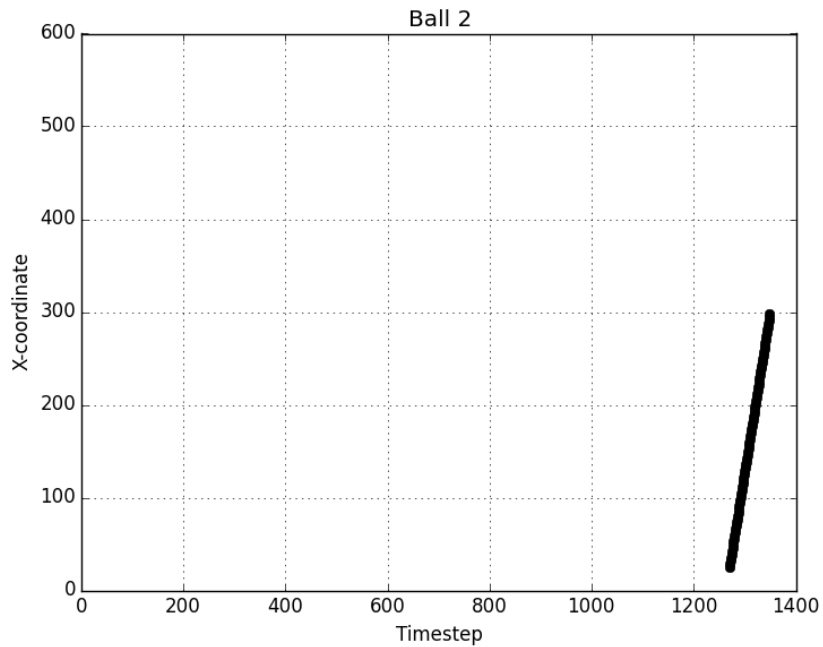
# Execution plots



# Execution plots



# Execution plots



# Future work

- Advanced scheduling of structure blocks
- Optimisation techniques
- Comparison to other methods (hybrid systems)

# Questions?