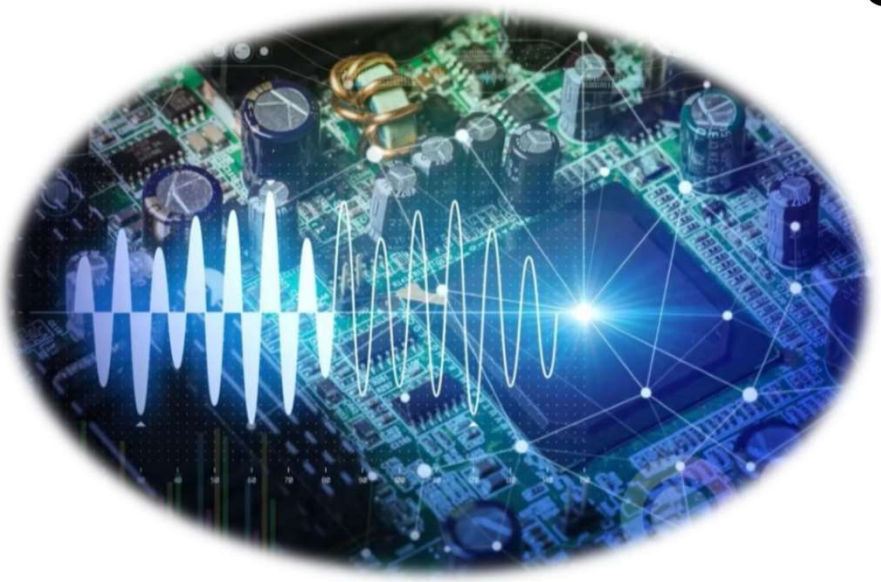
Analog Computing

Triangle



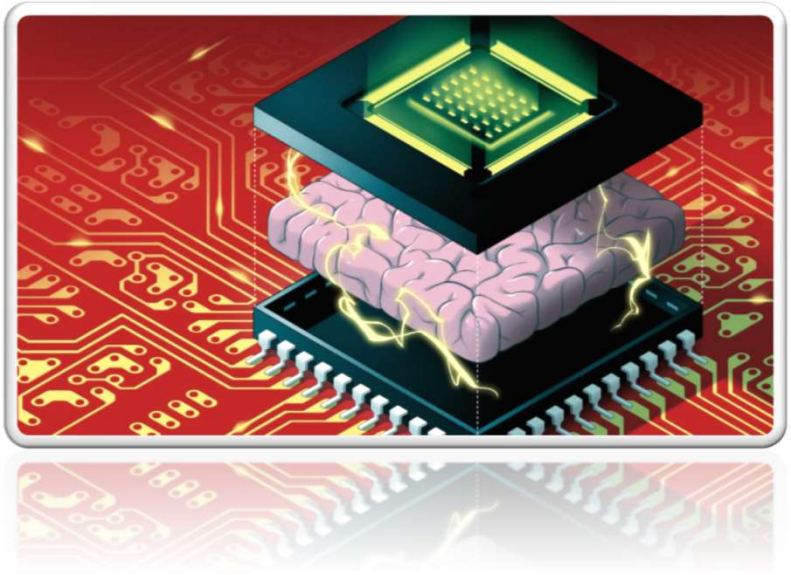
MSDL

Modelling, Simulation and Design Lab

Introduction

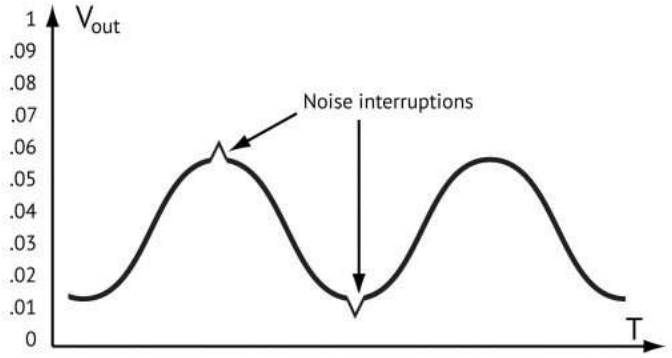
Analog Computers

- Use continuous physical quantities to represent and manipulate data
- More powerful and efficient for certain types of problems
- More sensitive to noise and disturbances
- Difficult to design and build
- Examples: human brain, biological systems, medical imaging

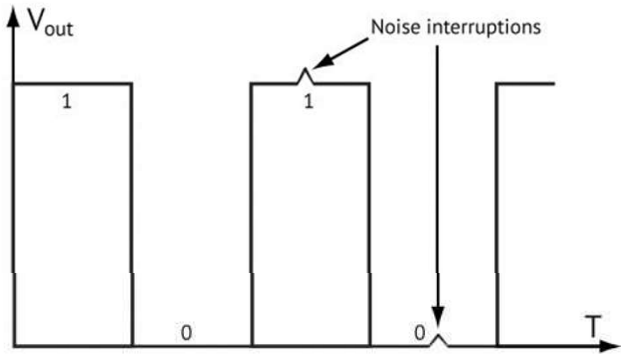


Digital Computers

- Use discrete binary values to represent and manipulate data
- More versatile and flexible
- Less sensitive to noise and disturbances
- Easier to design and build
- Examples: personal computers, smartphones, servers



Analog



Digital

Hardware in The Loop simulation

HiL simulation is a technique that uses a real-time simulator to test control strategies for embedded systems. The simulator replaces the physical system, so that the control strategy can be tested in a safe and controlled environment.

Mathematical model

Analog Computer for Hardware-in-the-Loop (HiL) Simulation

From dspace

Digital HiL systems are expensive and power-hungry.

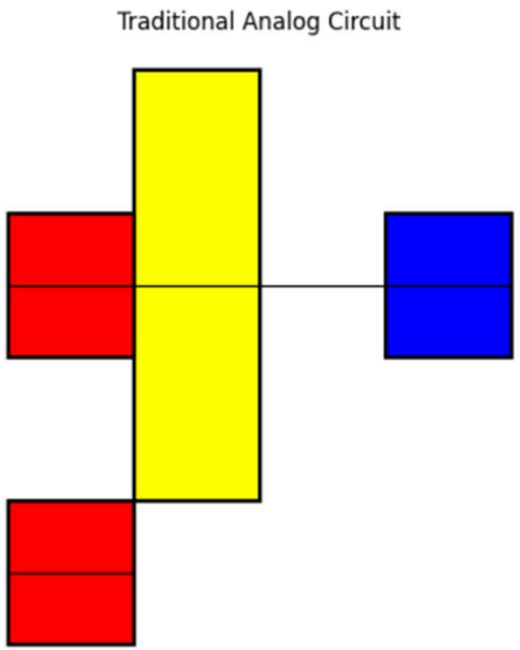
Analog: low power simulation, even of non-linear models.

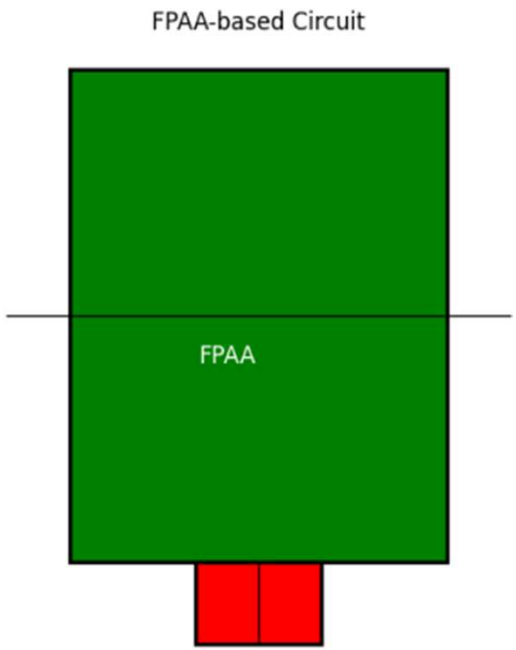
Analog Computing: Then and Now

1. Analog computers did not use numerical analysis.
2. Traditional analog computers were used to solve specific problems, not general ones.
3. Analog computers required a lot of manual work to find solutions.
4. Analog computation started with no real way to organize calculations.
5. Modern analog computation started in the 1980s, at the same time as neuromorphic computing
6. The lack of a computational framework
7. Without configurable and programmable systems, analog computing discussions are mostly theoretical.

Traditional Analog vs FPAA

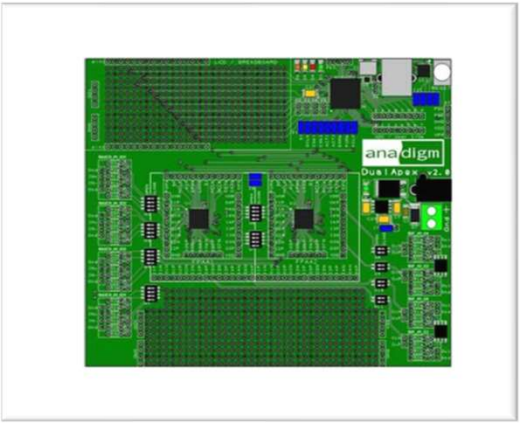
Feature	Traditional Analog Circuit	FPAA-based Circuit
Type	Fixed	Programmable
Components	Individual	Integrated circuit
Design	Simple	Complex
Applications	Simple	Complex
Cost	Low	High
Power consumption	Low	High
Speed (Propagation Delay)	Low	High



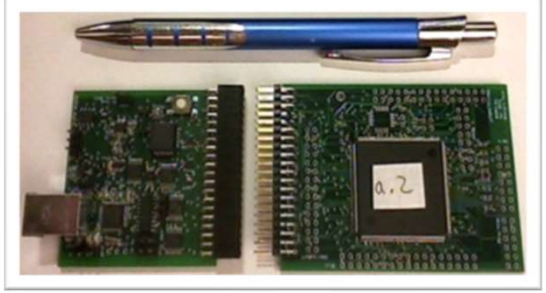


Field Programmable Analog Array (FPAA)

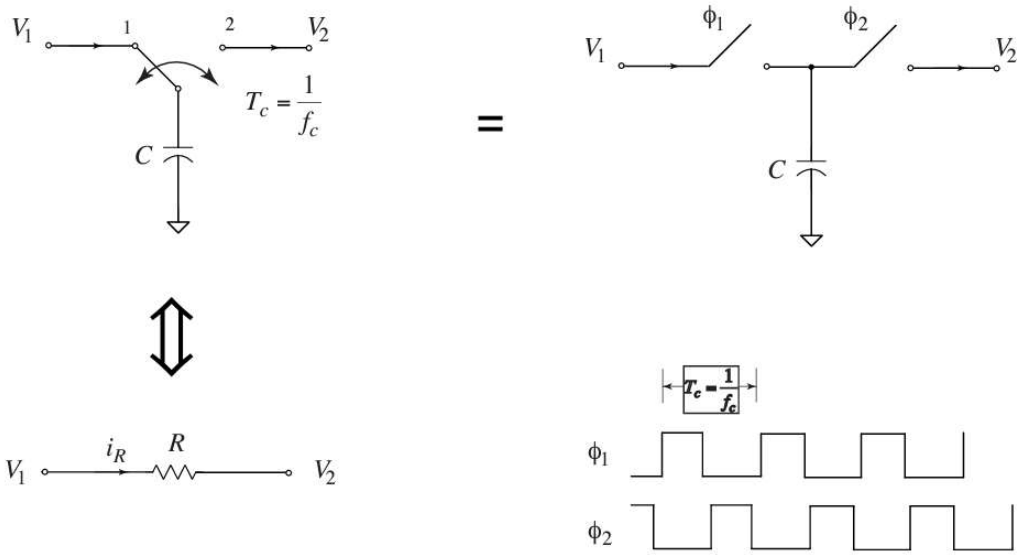
- Anadigm



- Hasler



Concept of Switched Capacitor



- ϕ_1, ϕ_2 is a two phase nonoverlapping clock

At position 1 the charge on C at steady state is $q_1 = CV_1$

At position 2 the charge on C at steady state is $q_2 = CV_2$

Assuming $V_1 > V_2$, the charge Δq transferred is

$$\Delta q = q_1 - q_2 = C(V_1 - V_2)$$

The current flowing will be on average

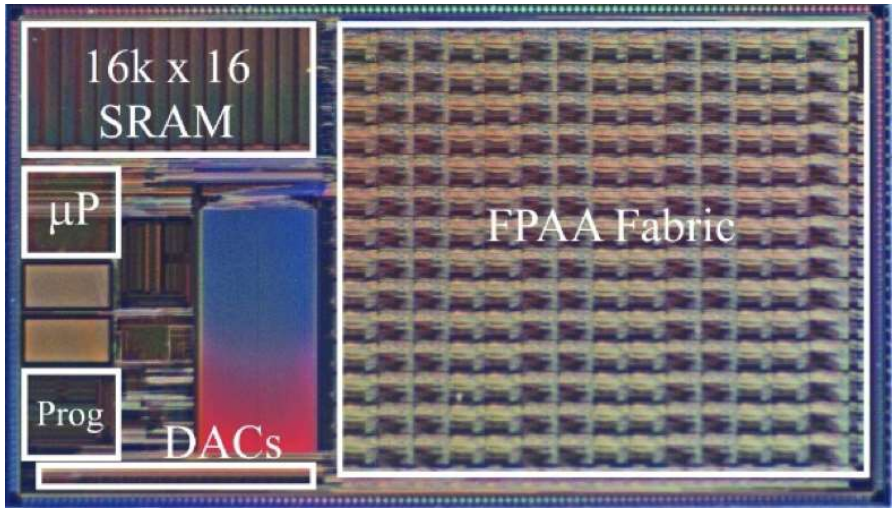
$$i(t) = \frac{\delta q(t)}{\delta t} = \lim_{\Delta T_c \to 0} \frac{\Delta q}{\Delta T_c} \cong \frac{C(V_1 - V_2)}{T_c} \quad (1)$$

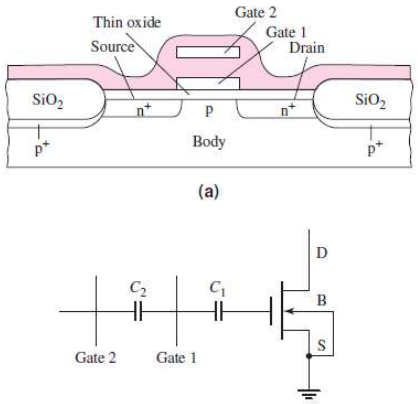
Consider now a resistance of value R connected to the same two sources V_1 & V_2. Then

$$i_R(t) = \frac{(V_1 - V_2)}{R} \quad (2)$$

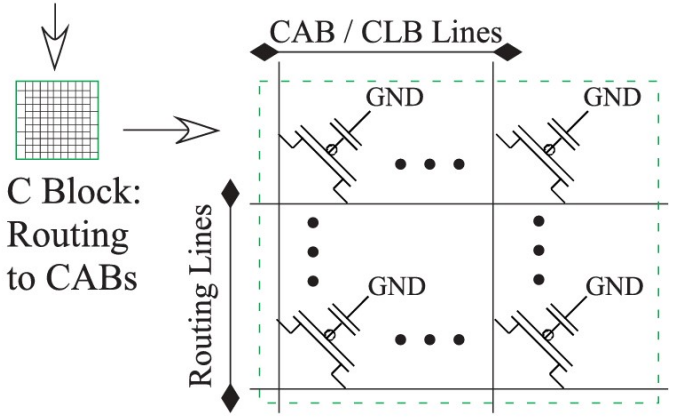
Equating (1) and (2) yields $R = \frac{T_c}{C} = \frac{1}{f_c C}$

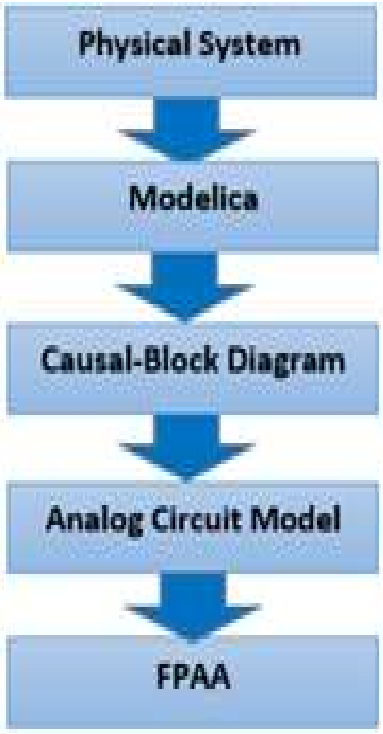
FPAA Structure





•Flexibility: The array of analog components can be reconfigured to perform different functions.
•Speed: The digital processor can be used to perform DSP operations on the signals that are processed by the array.
•Power efficiency: The analog components can be designed to consume less power than digital components.

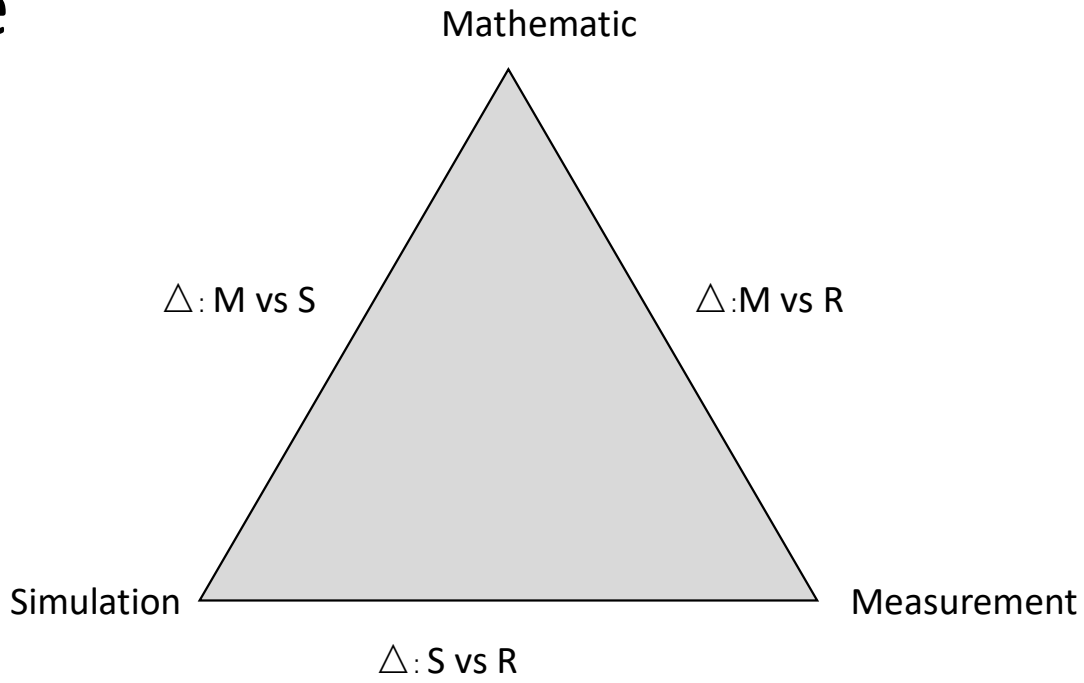




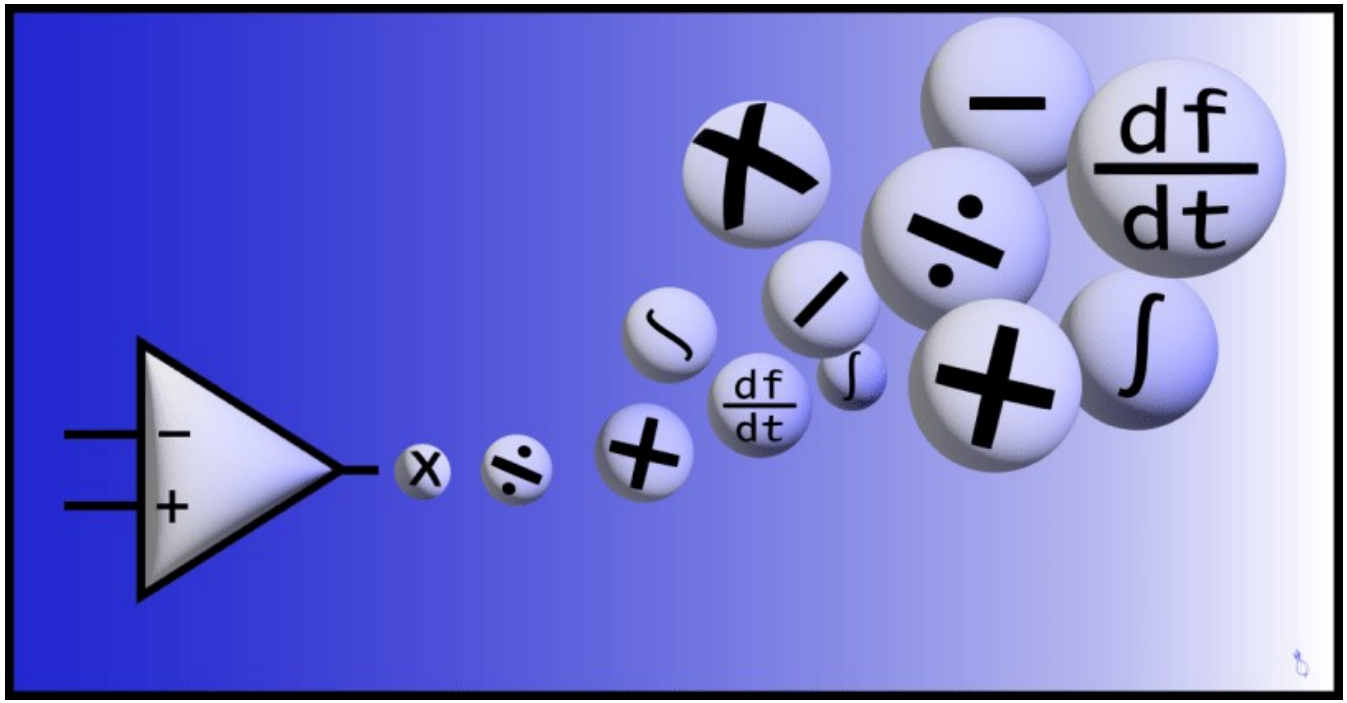
- Develop a compiler to automatically synthesize the connection topology of the analog electronic components in the FPAA.

- Study the trade-offs between numerical accuracy, real-time performance, and energy consumption.

Triangle



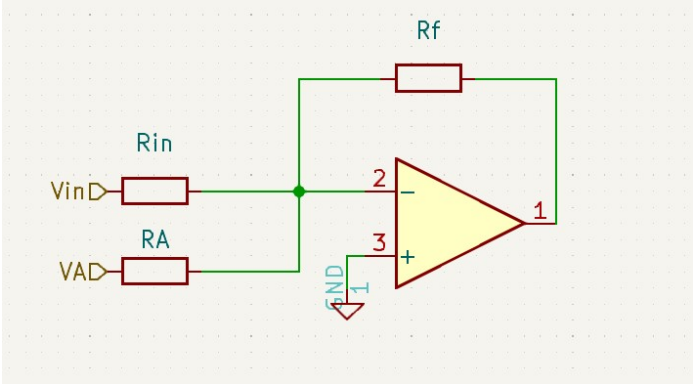
Basics



$$Vo = A + Vi$$

- vo=(-Rf/Rin)vin+(-Rf/Ra)VA

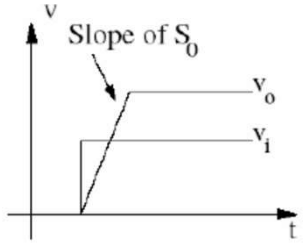
- Solution for Rf: [Ra*Rin*(-A - Vi)/(A*Rin + Ra*Vi)]
- Solution for Rin: [-Ra*Rf*Vi/(A*Ra + A*Rf + Ra*Vi)]
- Solution for Ra: [-A*Rf*Rin/(A*Rin + Rf*Vi + Rin*Vi)]



Design Consideration

- Voltage Limits VCC, VEE -VEE<Vo<Vcc
- Slew Rate : The maximum rate of changes of the output of an opamp is known as the slew rate (in units of V/s)

$$S_0 = \left.\frac{dv_o}{dt}\right|_{\max}$$



- Bandwidth: fsignal< bandwidth
- Boundary for Resistors
- Offset:
  Vo_real=Voffset+Vout

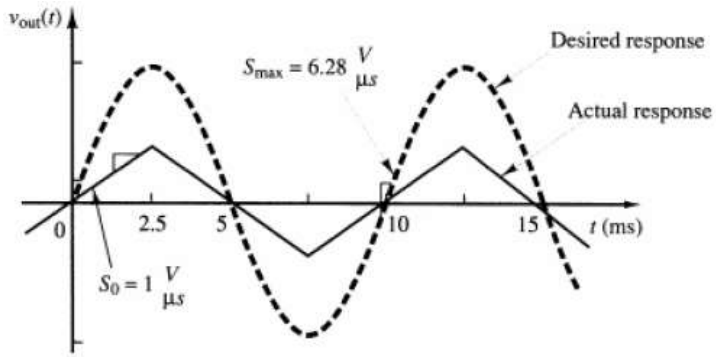
Slew rate example

- Consider an inverting amplifier, gain=10, built using an opamp with a slew rate of S_0=1V/μs.
- Input a sinusoid with an amplitude of V_i=1V and a frequency, ω.

$$v_i = V_i \cos(\omega t) \rightarrow v_o = -AV_i \cos(\omega t)$$

$$\frac{dv_o}{dt} = AV_i\omega \sin(\omega t) \rightarrow \left.\frac{dv_0}{dt}\right|_{\max} = AV_i\omega \le S_0$$

$$\left.\frac{dv_o}{dt}\right|_{\max} = 10\omega \le 10^6 \Rightarrow \omega \le 10^5$$

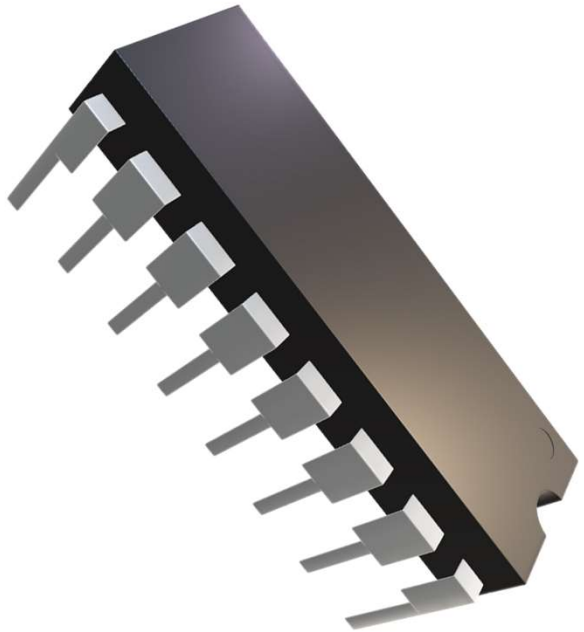


- For a sinusoid, the slew rate limit is of the form $AV_i\omega < S_0$.
- We can therefore avoid this non-linear behaviour by
  - decreasing the frequency (ω)
  - lowering the Amplifier gain (A)
  - lower the input signal amplitude (V_i)
- Typical values: 741C: 0.5V/μs, LF356: 50V/ μs, LH0063C: 6000V/ μs,

TL074

- High slew rate: 20 V/µs (TL07xH, typ)
- Low offset voltage: 1 mV (TL07xH, typ)
- Low offset voltage drift: 2 µV/°C
- Low power consumption: 940 µA/ch (TL07xH, typ)
- Wide common-mode and differential voltage ranges
- Low input bias and offset currents
- Low noise: V n = 18 nV/√ Hz
- Output short-circuit protection
- Low total harmonic distortion: 0.003% (typ)

- Wide supply voltage: ±2.25 V to ±20 V, 4.5 V to 40 V



Find Circuit Parameters

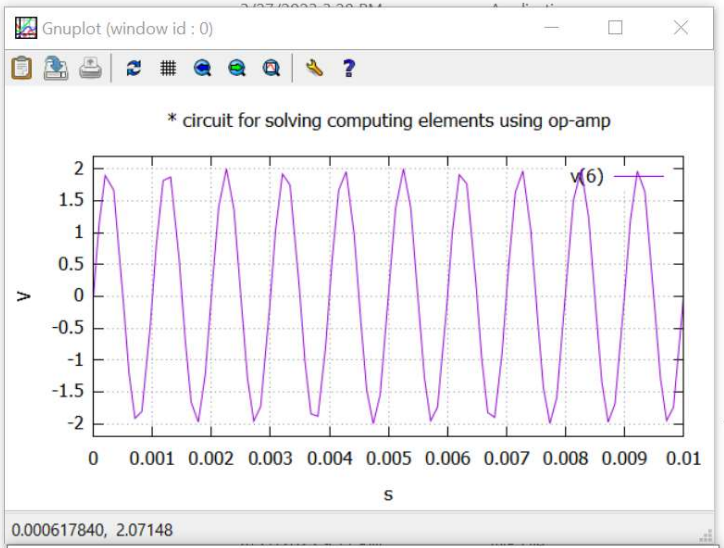
summnum.py

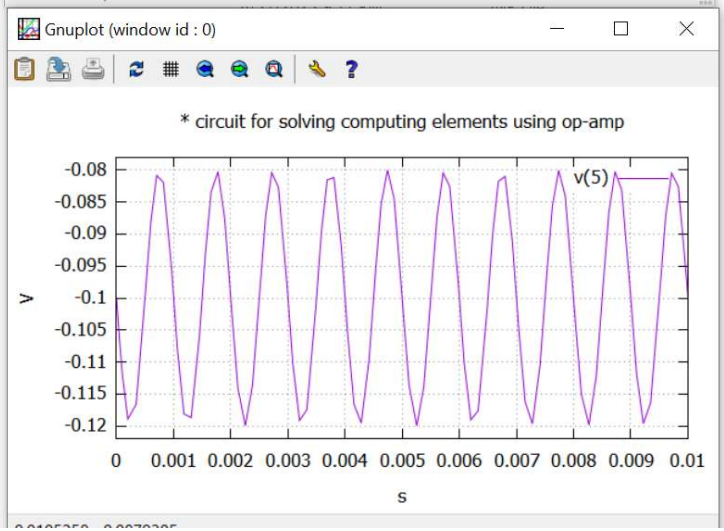
```
 Vo = 5
 Vi = 2
 A = 1
 V_offset = 1e-3  # 1mV offset
f_signal = 1e3  # input frequency in Hz

 Rf, Rin, Ra = x



 return -(Rf/Rin) * Vi - (Rf/Ra) * A + V_offset - Vo

Vcc = 10
Vee = -10

slew_rate = 20e-6  # 20 V/µs in V/s

bandwidth = 3e6  # 3 MHz in Hz

# Output voltage constraint

def constraint1(x):
    return Vcc - equation1(x)  # Vo<Vcc so Vcc - Vo >= 0

def constraint2(x):
    return equation1(x) - Vee  # Vo>-Vee so Vo +Vee >= 0
```

```
# Slew rate constraint
def constraint3(x):
    Rf, Rin, Ra = x
    max_dVo_dt = abs((Rf/Rin) * max_dvi_dt)
    return slew_rate - max_dVo_dt  #  >= 0

# Frequency constraint
def constraint4(x):
    Rf, Rin, Ra = x
    f_signal = 1e3  # 1 kHz
    return bandwidth - f_signal    #banwidth>f_signal

# Initial guesses for Rf, Rin, Ra
initial_guess = [1000, 1000, 1000]

# Bounds for Rf, Rin, Ra
bnds = [(100, 10000), (50, 10000), (50, 10000)]

# Constraint dictionary
con1 = {'type': 'ineq', 'fun': constraint1}
con2 = {'type': 'ineq', 'fun': constraint2}
con3 = {'type': 'ineq', 'fun': constraint3}

cons = [con1, con2, con3]

# Run the optimizer
solution = minimize(objective, initial_guess, bounds=bnds,
constraints=cons)

# Extract the solution
Rf, Rin, Ra = solution.x

print("Solution")scipy?
print("Rf:", Rf)
print("Rin:", Rin)
print("Ra:", Ra)
```

```
No solution found.

C:\Simulation_Python_FWO>python summnum.py
Solution
Rf: 100.0
Rin: 10000.0
Ra: 1000.0

C:\Simulation_Python_FWO>
```

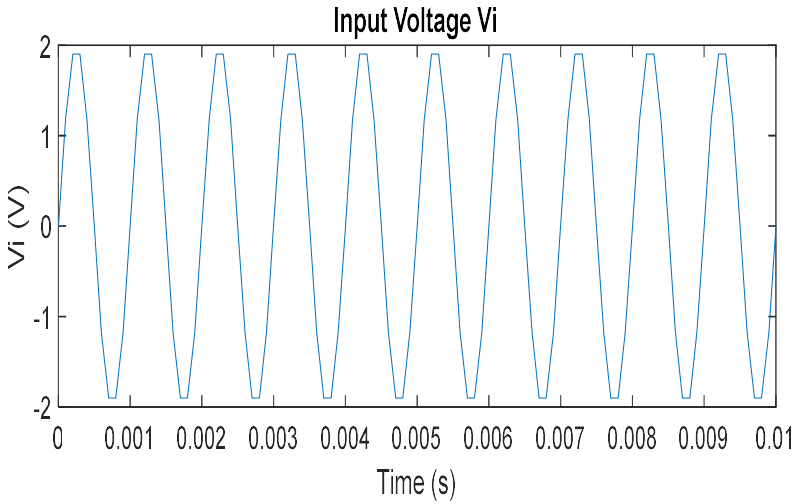
Simulation Result

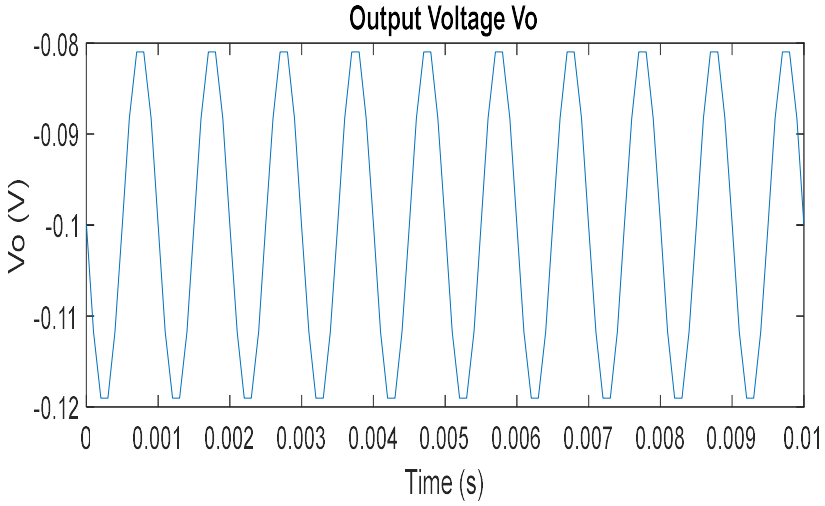




vo=(-Rf/Rin)vin+(-Rf/Ra)VA
=-0.01*2sint-0.1

Mathematic Result

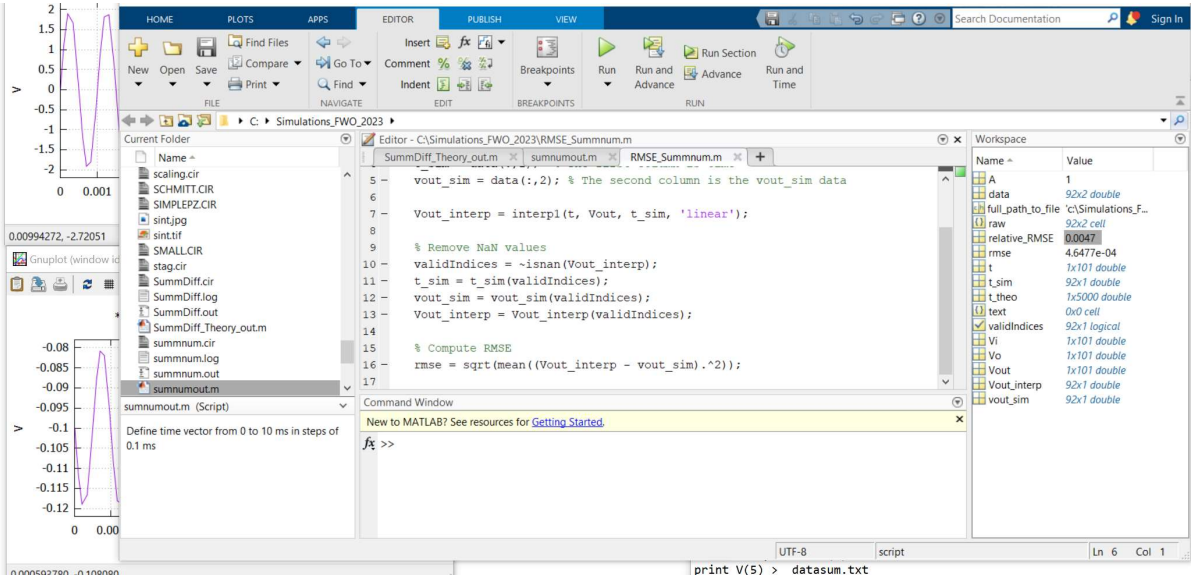




△ M vs S:

RMSE=4.6e-4

$$\text{RMSE}=\sqrt{\frac{1}{N}\sum_{i=1}^{N}(V_{omatlab,i}-V_{ongspice,i})^2}$$

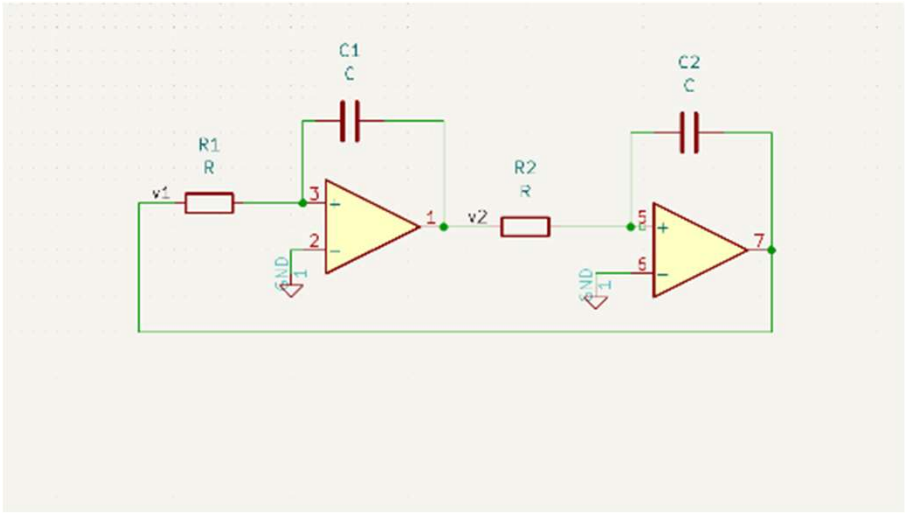


Under study

- $Vo = A \times Vi$
- $Vo = -A \times Vi$
- $Vo = A \times V1i + B \times V2i$
- $Vo = A + B \times V1i \times V2i$
- $Vo = A + B \times \frac{V1i}{V2i}$
- $Vo = A + B \times \frac{dVi}{dt}$ $\qquad\qquad Vi(0) = C$

dx2/dt2=-x(t), x(0)=0, dx/dt(0)=1

- v1(t)=x(t), dv1(t)/dt=dx/dt
- v2(t)=dx/dt, dv2(t)/dt=d2x/dt2=-x(t)=-v1(t)
- Considering 1 stage for 1 derivative:
- vout(t)=-1＼RC∫Vin(t)dt
- $v_2(t)=1＼R_1C_1\int v_1(t)dt$
- $v_1(t)=1＼R_2C_2\int v_2(t)dt$



Design Consideration

Frequency Response:

Cutoff frequency of an integrator: fc=1/2πRC

Op-Amp Limitations:

Slew Rate

fmax= SR/2πv=20/2.π.2=1.5 MHz

Assumption: f=10Hz

R=100 kohm C= 1/2πRfc=0.159uF (C=150nf is a standard value)

Input Bias Current: Op-amps have a small DC current flowing into their inputs. very large resistances create a significant voltage drop .

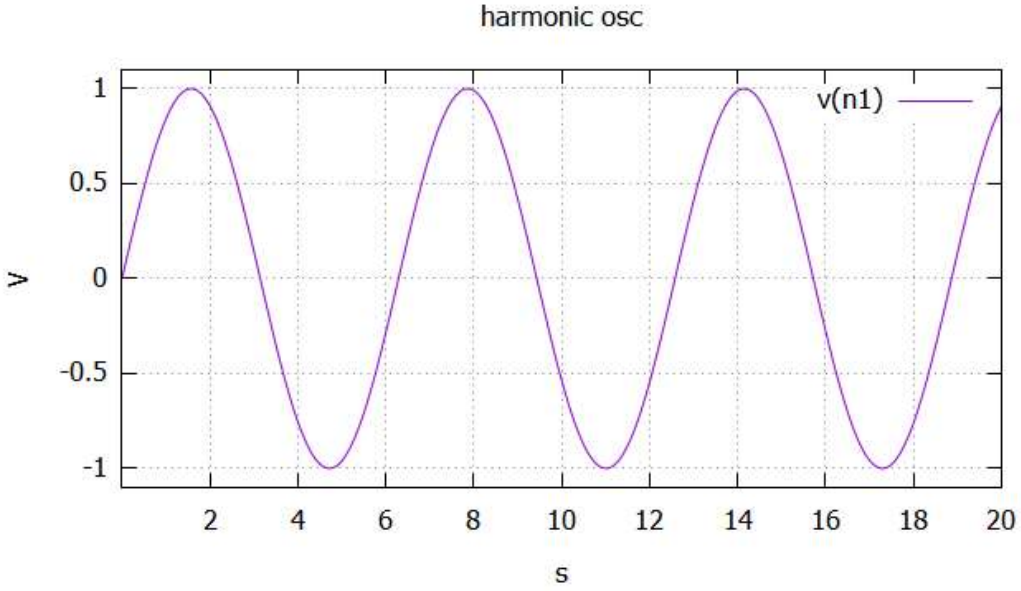
Noise: High resistor values leads to more thermal noise

Capacitors leads to dielectric noise (compared with thermal noise not a concern)

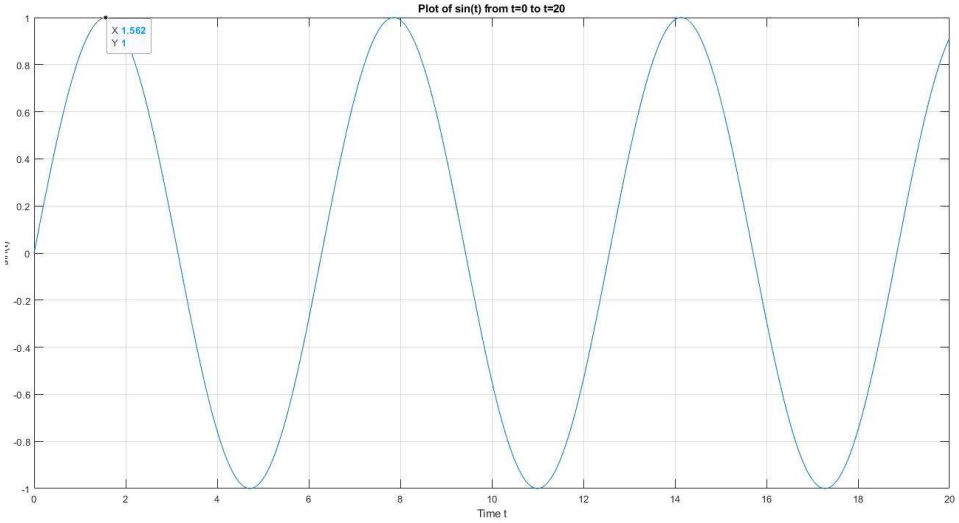
Physical Size and Cost:

Larger capacitor values leads to larger sizes and more expensive.

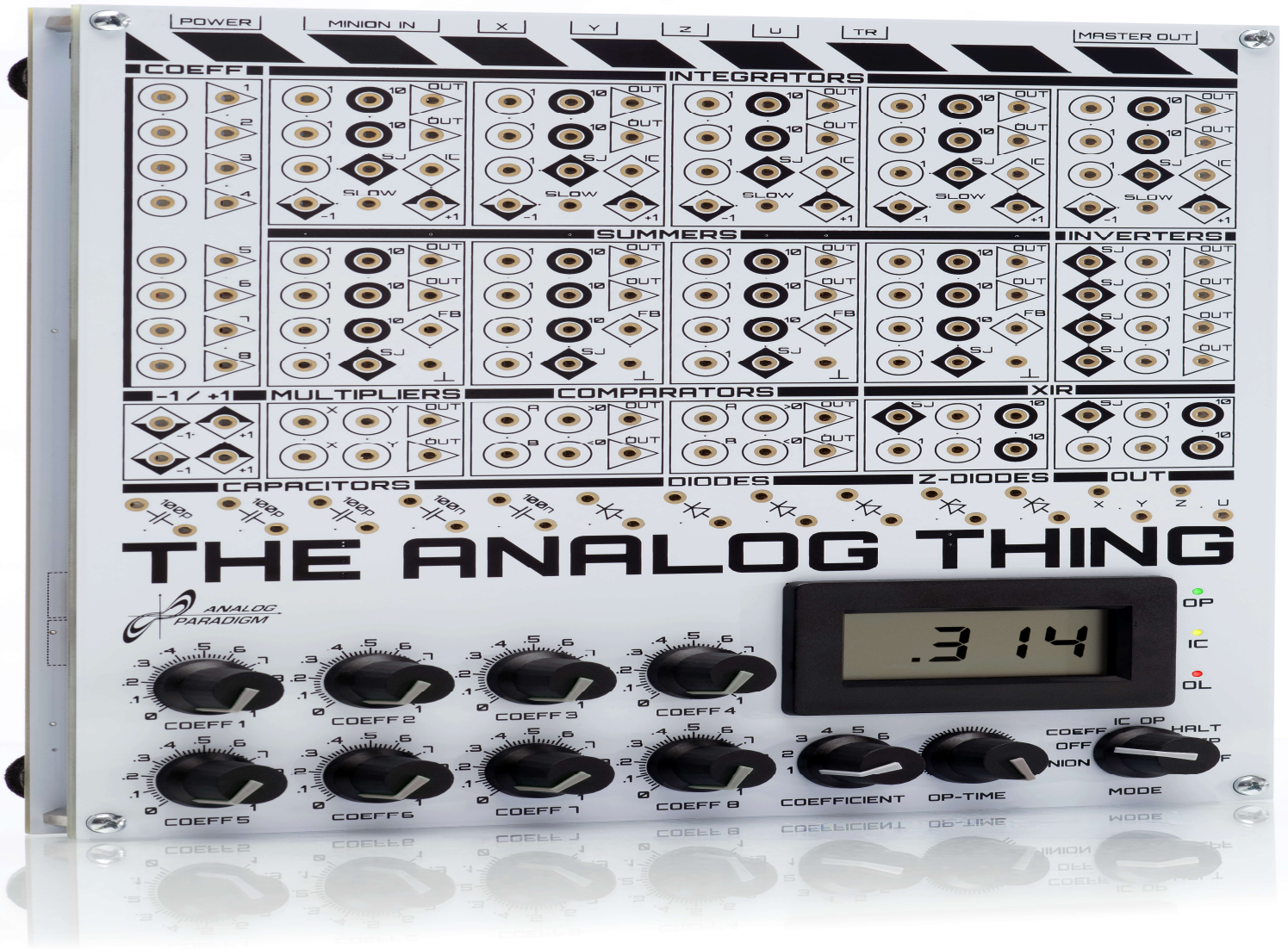
Simulation Result



Mathematic Result

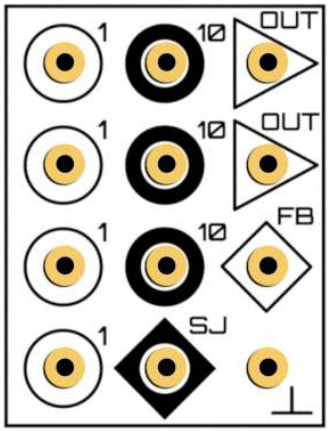


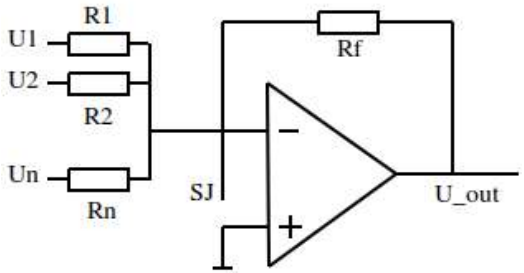
RMSE=0.0067

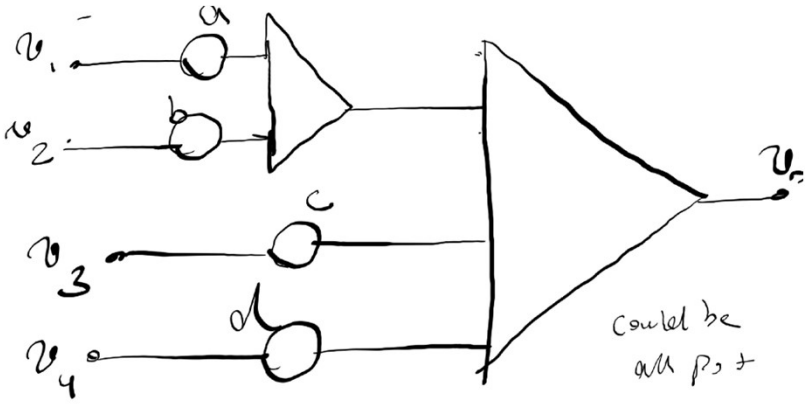

POWER
MINION IN
X
Y
Z
U
TR
MASTER OUT
COEFF
INTEGRATORS
SUMMERS
INVERTERS
-1 / +1
MULTIPLIERS
COMPARATORS
XIR
CAPACITORS
DIODES
Z-DIODES
OUT
THE ANALOG THING
ANALOG PARADIGM
.314
OP
IC
OL
COEFF 1
COEFF 2
COEFF 3
COEFF 4
COEFF 5
COEFF 6
COEFF 7
COEFF 8
COEFFICIENT
OP-TIME
MODE
HALT

Summation-Subtraction

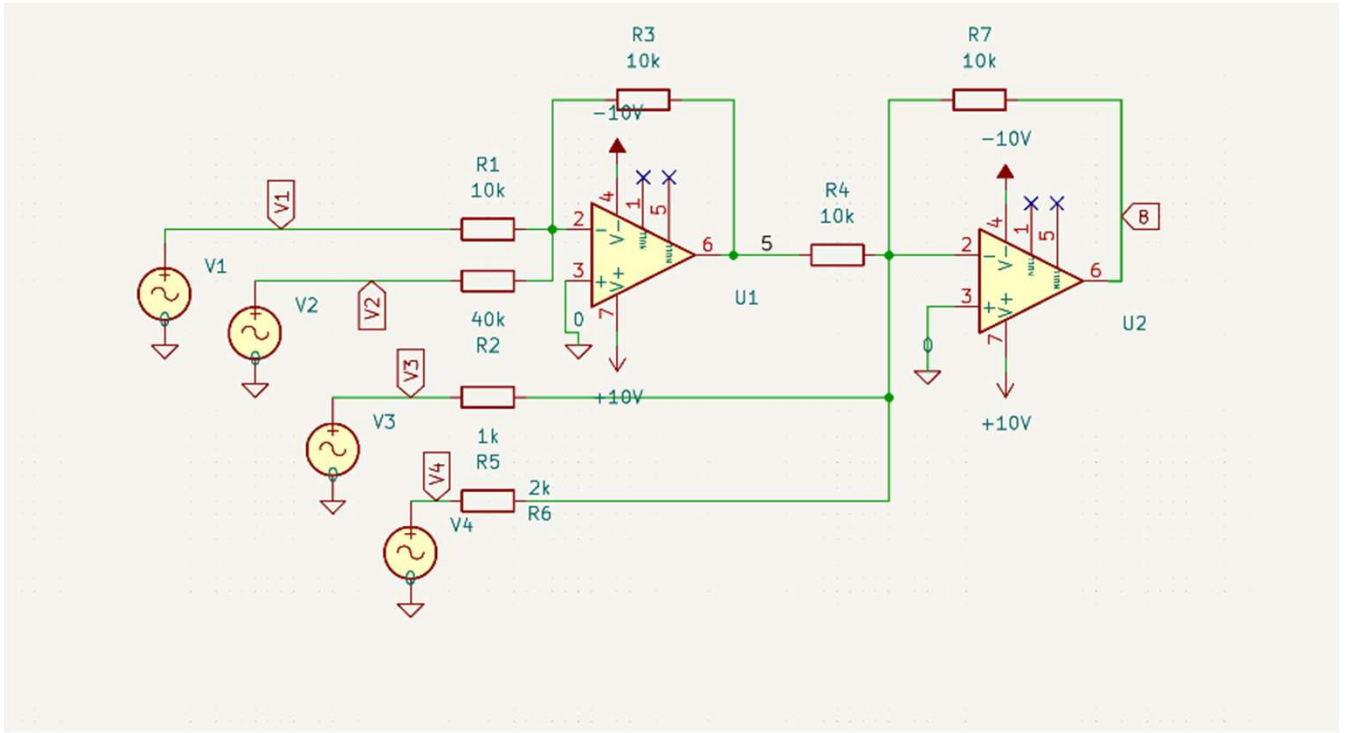
THAT board:







Vo=av1+bv2-cv3-dv4


R3
10k
R7
10k
−10V
−10V
R1
10k
R4
10k
V1
V1
V2
V2
40k
R2
U1
5
U2
B
V3
V3
+10V
+10V
1k
R5
V4
2k
R6
V4
0
0
0
1
2
3
4
5
6
7

$$\begin{cases} V_8 = \frac{R_7 R_3}{R_4 R_1} V_1 + \frac{R_7 R_3}{R_4 R_2} V_2 - \frac{R_7}{R_5} V_3 - \frac{R_7}{R_6} V_4 \\ V_8 = aV_1 + bV_2 - cV_3 - dV_4 \end{cases} \qquad a=1,\ b=0.25,\ c=10,\ d=5$$

$$\frac{R_7 R_3}{R_4 R_1} = a \rightarrow R_1 = \frac{R_3 R_7}{a R_4} \rightarrow \frac{R_1}{R_2} = \frac{b}{a}$$

$$\frac{R_7 R_3}{R_4 R_2} = b \rightarrow R_2 = \frac{R_3 R_7}{b R_4}$$

$$\frac{R_7}{R_5} = c \rightarrow R_5 = \frac{R_7}{c}$$

$$\frac{R_7}{R_6} = d \rightarrow R_6 = \frac{R_7}{d}$$

if assume: $R_7 = 10^k \rightarrow R_5 = 1^k$, $R_6 = 2^k$

$$\frac{R_1}{R_2} = 0.25$$

if $R_1 = 10^k \rightarrow R_2 = 40^k$, $R_3 = \frac{a R_4 R_1}{R_7} = 10^k$

if $R_4 = 10^k$

Scaling Circuit

```
x1  1 2 3 4 5 TL074
R1 2 5 50k
R2 2 w 50k
Apot1 6 w 0 potmod1
vcc 3 0 5v
vdd 4 0 -5v
vin1 6 0 dc 0 sin(0 0.2 500hz)
vin2 7 0 dc 0 sin(0 0.166 500hz)
v+ 1 0 0
R3 2 z 50k
Apot2 7 z 0 potmod2
.model potmod1 potentiometer(position=0.1325 r=1k log=FALSE log_multiplier=1)
*Position: 0.5*5/8
.model potmod2 potentiometer(position=0.1875 r=1k log=FALSE log_multiplier=1)
*Position: 0.5*3/8
```

Vin1 = 0.2V * sin(2πft)
Vin2 = 0.166V * sin(2πft)
Potentiometer1 position = 0.1325 (Vin1 is scaled by this factor)
Potentiometer2 position = 0.1875 (Vin2 is scaled by this factor)
The operational amplifier (TL074) is configured in an inverting mode.
t = 0.5ms.
Vin1(t) = 0.2V * sin(2π500Hz0.0005s) = 0.2V Vin2(t) = 0.166V * sin(2π500Hz0.0005s) = 0.166V
Vw1 = Vin1 * potentiometer1_position = 0.2V * 0.1325 = 0.0265V
Vw2 = Vin2 * potentiometer2_position = 0.166V * 0.1875 = 0.031125V
V(5) = - (Vw1 + Vw2) = - (0.0265V + 0.031125V) = -0.057625V or -57.625mV

Multiplication with constant

Vin = 1V * sin(2 * π * 500Hz * 0.0005s)=1v

A = 1 + (R1 / R2)

A = 1 + (50kΩ / 50kΩ) = 2

V(5) = A * Vin*0.35 0.35 is the position of potentiometer

V(5) = 2 * 0.35V = 0.7V

V(5)=0.6632 ,

Percent error = (|0.7V - 0.6632V| / 0.7V) * 100%

Percent error ≈ 5.26%